

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2002-134661

(43)Date of publication of application : 10.05.2002

(51)Int.CI.

H01L 23/28

H01L 21/56

H01L 23/12

(21)Application number : 2000-326602

(71)Applicant : MATSUSHITA ELECTRIC IND CO LTD

(22)Date of filing : 26.10.2000

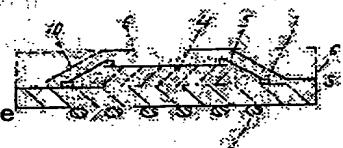
(72)Inventor : FUJIMOTO HIROAKI
SAWARA RYUICHI
NANO MASANORI
FUKUDA TOSHIYUKI
NOMURA TORU

(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To solve the lightweight problem even in a BGA type semiconductor device in accordance with the desire of the small size and lightweight of electronic equipment.

SOLUTION: The semiconductor device is composed of a wiring board 3 having a wiring electrode 1 on the upper face and having a ball electrode 2 on the bottom face, a semiconductor chip 4 mounted on the upper face of the wiring board 3, a metal fine wire 5 connecting the semiconductor chip 4 and the wiring electrode 1 of the wiring board 3, and an insulation sealing resin 6 sealing the upper face of the wiring board 3. The sealing resin 6 is eliminated on the peripheral part of the upper face of the sealing resin 6, which has an oblique part 10, in the case that the volume of the sealing resin 6 of a virtual substantially rectangular shape is 100%, the 20% or more sealing resin thereof is eliminated. Thereby the sealing resin amount of the upper face peripheral part is remarkably reduced, the weight is decreased, and the lightweight BGA type semiconductor device is realized.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.

2. **** shows the word which can not be translated.

3. In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] A wiring substrate with the external electrode electrically connected with said wiring electrode on the wiring electrode and the base on the top face, The metal thin line which connected the semiconductor chip with which the base was carried in said wiring substrate by pasting up, and the electrode of said semiconductor chip and the wiring electrode of said wiring substrate, It is the semiconductor device with which it consists of closure resin which closed the top face of said wiring substrate, and the top-face periphery of said closure resin is characterized by deleting closure resin and having the oblique side.

[Claim 2] The top-face periphery of closure resin is a semiconductor device according to claim 1 characterized by deleting closure resin, having an oblique side and thin closure resin remaining in the top face of a wiring substrate.

[Claim 3] The semiconductor device according to claim 1 characterized by deleting the closure resin more than 20 of them [%], and having the oblique side when the volume of the closure resin of an abbreviation rectangular parallelepiped configuration is set to 100 [%].

[Claim 4] A wiring substrate with the external electrode electrically connected with said wiring electrode on the wiring electrode and the base on the top face, The metal thin line which connected the semiconductor chip with which the base was carried in said wiring substrate by pasting up, and the electrode of said semiconductor chip and the wiring electrode of said wiring substrate, It is the semiconductor device which consists of closure resin which closed said some of semiconductor chips of the top face of said wiring substrate, and the field of a metal thin line, and is characterized by exposing top faces other than the connection field of the metal thin line of said semiconductor chip from closure resin.

[Claim 5] The top-face periphery of closure resin is a semiconductor device according to claim 4 characterized by deleting closure resin and having the oblique side.

[Claim 6] The top-face periphery of closure resin is a semiconductor device according to claim 4 characterized by deleting closure resin, having an oblique side and thin closure resin remaining in the top face of a wiring substrate.

[Claim 7] The semiconductor device according to claim 4 characterized by deleting the closure resin more than 40 of them [%] when the volume of the closure resin of an abbreviation rectangular parallelepiped configuration is set to 100 [%].

[Claim 8] The process which prepares for a wiring electrode and a base a wiring substrate with the external electrode electrically connected with said wiring electrode in the semiconductor chip unit carried at least on the top face, The process which pastes up two or more semiconductor chips to the top face of said wiring substrate, The process which connects respectively the electrode of said semiconductor chip, and the wiring electrode of said wiring substrate electrically with a metal thin line, The process which closes the enclosure of each semiconductor chip of the top face of said wiring substrate, and a metal thin line by closure resin at least, and forms the closure resin of an abbreviation rectangular parallelepiped configuration, As opposed to the closure resin side of the cutting field of each semiconductor chip unit on said wiring substrate The process which carries out grinding of said closure

resin, deletes it with the 1st broad blade, and makes the periphery of the top face of closure resin a bevel configuration in a cross-section configuration. The manufacture approach of the semiconductor device characterized by having the process which cuts said wiring substrate with the 2nd blade with width of face narrower than said 1st blade, divides into each semiconductor chip unit, and obtains a semiconductor device.

[Claim 9] As opposed to the closure resin side of the cutting field of each semiconductor chip unit on a wiring substrate At the process which carries out grinding of said closure resin, deletes it with the 1st broad blade, and makes the periphery of the top face of closure resin a bevel configuration in a cross-section configuration The manufacture approach of the semiconductor device according to claim 8 characterized by deleting the closure resin more than 20 of them [%] when the volume of the closure resin of an abbreviation rectangular parallelepiped configuration is set to 100 [%].

[Claim 10] The process which prepares for a wiring electrode and a base a wiring substrate with the external electrode electrically connected with said wiring electrode in the semiconductor chip unit carried at least on the top face, The process which pastes up two or more semiconductor chips to the top face of said wiring substrate, The process which connects respectively the electrode of said semiconductor chip, and the wiring electrode of said wiring substrate electrically with a metal thin line, The process which closes the enclosure of each semiconductor chip of the top face of said wiring substrate, and a metal thin line by closure resin at least, It consists of a process which cuts said wiring substrate, divides into each semiconductor chip unit, and obtains a semiconductor device. The process which closes the enclosure of each semiconductor chip of the top face of said wiring substrate, and a metal thin line by closure resin at least The manufacture approach of the semiconductor device characterized by being the process which closes where a web material is stuck on the top face other than the field where the metal thin line of said semiconductor chip connected, is exposed from closure resin and closes top faces other than the connection field of the metal thin line of said semiconductor chip.

[Claim 11] It receives in the closure resin side of the cutting field of each semiconductor chip unit on a wiring substrate after the process which closes the enclosure of each semiconductor chip of the top face of said wiring substrate, and a metal thin line by closure resin at least. With the 1st broad blade, carry out grinding of said closure resin, delete it, and it has the process which makes the periphery of the top face of closure resin a bevel configuration in a cross-section configuration. The manufacture approach of the semiconductor device according to claim 10 characterized by having the process which cuts said wiring substrate with the 2nd blade with width of face narrower than said 1st blade, divides into each semiconductor chip unit, and obtains a semiconductor device next.

[Translation done.]

* NOTICES *

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.**** shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] The closure of the top face of the substrate in which the semiconductor chip was carried is carried out by closure resin, and this invention relates to the semiconductor device which realized lightweight-ization which can be equivalent to especially small lightweight-ization of electronic equipment, and its manufacture approach about the semiconductor device and its manufacture approach of the ball grid array (BGA) type with which the ball electrode was attached to the substrate base.

[0002]

[Description of the Prior Art] As an area array type semiconductor device, the closure of the top face of the substrate in which the semiconductor chip was carried is carried out by closure resin, and there is a semiconductor device of the BGA type with which the ball electrode was attached to the substrate base.

[0003] Hereafter, it explains, referring to a drawing about the conventional semiconductor device.

Drawing 23, drawing 24, and drawing 25 are drawings showing the semiconductor device of a BGA mold as a conventional semiconductor device, and drawing 23 is [a bottom view and drawing 25 of a top view and drawing 24] the sectional views of one A-A of drawing 23.

[0004] As shown in drawing 23, drawing 24, and drawing 25, the conventional semiconductor device The external pad electrode which has the wiring electrode 1 on the top face, and was electrically connected to it inside the wiring electrode 1 and substrate on the base (not shown), The semiconductor chip 4 carried on the external pad electrode in the bonding location of the top face of the wiring substrate 3 with the ball electrode 2, and the wiring substrate 3, It consists of a metal thin line 5 which connected electrically the semiconductor chip 4 and the wiring electrode 1 of the wiring substrate 3, and insulating closure resin 6 which closed the top face of the wiring substrate 3. In the conventional semiconductor device, as an appearance configuration, each side face has a perpendicular field and is making the shape of a rectangle as a whole. In addition, this appearance configuration is a configuration on a manufacture process.

[0005] Moreover, in the conventional semiconductor device, the ball electrode 2 attached to the wiring substrate 3 is a solder ball, and is attached for the high connection dependability in the case of secondary mounting to a mounting substrate. Moreover, in the arrangement, it is arranged in the shape of a grid to the base of the wiring substrate 3.

[0006] Moreover, as another gestalt of the conventional semiconductor device, as shown in the sectional view of drawing 26, in consideration of the dependability at the time of secondary mounting, the oblique side section 7 is formed in the periphery of the top face of the closure resin 6 which closed the top face of the wiring substrate 3, and there is also a semiconductor device of the BGA mold which deleted the corner.

[0007] Next, the manufacture approach of the conventional semiconductor device is explained. Drawing 27 – drawing 30 are drawings showing the manufacture approach of the conventional semiconductor device, drawing 27 (a) is a top view, drawing 27 (b) is a bottom view, and drawing 28 – drawing 30 are top views. Moreover, in drawing 29 and drawing 30, the part is considered as the top view which penetrated the internal structure.

[0008] As first shown in drawing 27 (a) and (b), it consists of insulating resin and the large-sized wiring substrate 3 for semiconductor chip loading equipped with the external pad electrode 8 which was equipped with two or more wiring electrodes 1, and was electrically connected inside the wiring electrode 1 and substrate at the base at the top face in the semiconductor chip unit to carry is prepared. The external pad electrode 8 is a part to which a ball electrode is attached at a back process. Moreover, the wiring substrate 3 prepared here carries two or more semiconductor chips in one substrate, and prepares the large-sized substrate for dividing into the semiconductor device of each [after that]. It is break Rhine at the time of the field shown with the broken line being divided into each semiconductor device among drawing 27. Moreover, in drawing 27 (a), the central field surrounded with

each wiring electrode 1 constitutes the bonding location in which a semiconductor chip is carried. [0009] Next, as shown in drawing 28 (a), the wiring substrate 3 as shown in drawing 27 is prepared, as shown in drawing 28 (b), to each bonding location of the top face of the wiring substrate 3, respectively, adhesion immobilization is carried out with adhesives and a semiconductor chip 4 is carried.

[0010] Next, as shown in drawing 29 (a), the electrode pad (not shown) of the semiconductor chip 4 carried on the wiring substrate 3 and the wiring electrode 1 prepared in the top face of the wiring substrate 3 are electrically connected with the metal thin line 5.

[0011] And as shown in drawing 29 (b), the whole top-face surface of the wiring substrate 3 is closed with closure resin 6. A transfer mold performs the top-face closure by this closure resin 6. In addition, the broken line shows the condition of having penetrated each configuration of the wiring electrode 1 and a semiconductor chip 4 in drawing 29 (b), and the metal thin line is omitted.

[0012] And as shown in drawing 30, when a top face cuts for every unit of each semiconductor chip 4 with a rotation blade to the wiring substrate 3 by which the whole surface closure was carried out by closure resin 6, the piece[of an individual]-ized semiconductor device 9 is obtained. Since it is the same as that of the structure shown in drawing 23, drawing 24, and drawing 25 as structure of the semiconductor device 9 obtained here, illustration is omitted.

[0013] In the case of cutting with a rotation blade, a piece of individual-like semiconductor device can be obtained with a sufficient precision here by cutting along break Rhine for division established in the wiring substrate 3. Usually, the dicing facility using the blade of the width of face of 20 [μm] extent used by the semi-conductor production process performs division with this rotation blade. Moreover, in case division cutting is carried out at the piece of an individual, it may cut from the case [where it cuts from the base side of the wiring substrate 3], and closure resin 6 side on the top face of a substrate.

[0014] To each piece[of an individual]-ized semiconductor device, a solder ball is attached to the external pad electrode of the base of the wiring substrate 3 as a back process, a ball electrode is formed, and an external terminal is constituted.

[0015] The semiconductor device of a BGA mold was conventionally manufactured using the large-sized substrate in which two or more semiconductor chips can be carried according to the process of performing loading, electric connection, and a resin seal to the substrate, and dividing a semiconductor chip into it by package cutting at the piece of an individual at last, as mentioned above.

[0016]

[Problem(s) to be Solved by the Invention] however, by said conventional semiconductor device and its conventional manufacture approach Since the semiconductor chip was carried in the substrate, the resin seal was performed after electric connection using the large-sized substrate in which two or more semiconductor chips can be carried and the semiconductor device of a BGA mold was finally manufactured according to the process of carrying out blade cutting, to the piece of an individual, As a description on the manufacture, the appearance configuration of the obtained semiconductor device was what has the field where each side face is perpendicular, and is making the shape of a rectangle as a whole. Therefore, as a semiconductor device, there were many amounts of volume of closure resin, and lightweight-ization of whole weight was not able to be attained. Moreover, although there was structure which deleted each corner of the top-face periphery of the closure resin of a semiconductor device as a conventional semiconductor device, the purpose of this corner deletion was not a thing to the extent that it is the crack of the corner at the time (secondary mounting) of mounting of a mounting substrate, and the purpose which prevents KAKE, it is the range of 5 [%] extent as an amount of reduction of closure resin and a semiconductor device can be contributed to lightweight-ization.

[0017] This invention raises the dependability at the time of secondary mounting to a mounting substrate etc. while manufacturing a semiconductor device, without causing decline in manufacture effectiveness, and it aims at offering the semiconductor device which can attain lightweight-ization sharply as a semiconductor device further paying attention to the weight of closure resin, and its manufacture approach. The weight of the closure resin about which we are anxious in the semiconductor

device of the BGA mold of stack structure with which laminating loading of two or more semiconductor chips was carried out on the wiring substrate especially in ***** is reduced, and it aims at offering the semiconductor device which realizes lightweight-ization which can be equivalent to small lightweight-ization of electronic equipment, and its manufacture approach.

[0018]

[Means for Solving the Problem] In order to solve said conventional technical problem the semiconductor device of this invention A wiring substrate with the external electrode electrically connected with said wiring electrode on the wiring electrode and the base on the top face, The metal thin line which connected the semiconductor chip with which the base was carried in said wiring substrate by pasting up, and the electrode of said semiconductor chip and the wiring electrode of said wiring substrate, Consisting of closure resin which closed the top face of said wiring substrate, the top-face periphery of said closure resin is a semiconductor device which closure resin is deleted and has the oblique side.

[0019] Specifically, the top-face periphery of closure resin is a semiconductor device with which closure resin is deleted, it has an oblique side, and thin closure resin remains in the top face of a wiring substrate.

[0020] Moreover, when the volume of the closure resin of an abbreviation rectangular parallelepiped configuration is set to 100 [%], it is the semiconductor device which the closure resin more than 20 of them [%] is deleted, and has the oblique side.

[0021] Moreover, a wiring substrate with the external electrode which connected the semiconductor device of this invention with said wiring electrode electrically on the wiring electrode and the base on the top face, The metal thin line which connected the semiconductor chip with which the base was carried in said wiring substrate by pasting up, and the electrode of said semiconductor chip and the wiring electrode of said wiring substrate, Consisting of closure resin which closed said some of semiconductor chips of the top face of said wiring substrate, and the field of a metal thin line, top faces other than the connection field of the metal thin line of said semiconductor chip are semiconductor devices exposed from closure resin.

[0022] Specifically, the top-face periphery of closure resin is a semiconductor device which closure resin is deleted and has the oblique side.

[0023] Moreover, the top-face periphery of closure resin is a semiconductor device with which closure resin is deleted, it has an oblique side, and thin closure resin remains in the top face of a wiring substrate.

[0024] Moreover, when the volume of the closure resin of an abbreviation rectangular parallelepiped configuration is set to 100 [%], it is the semiconductor device with which the closure resin more than 40 of them [%] is deleted.

[0025] As said configuration, when the oblique side section is constituted, the amount of closure resin is reduced sharply and the volume of the closure resin of the abbreviation rectangular parallelepiped configuration of imagination is set to 100 [%] by carrying out the bevel cut of the top-face periphery of closure resin, the semiconductor device of this invention deletes the closure resin more than 20 of them [%], reduces weight by reduction of the amount of closure resin, and can realize a lightweight semiconductor device as a whole.

[0026] The process which prepares for a wiring electrode and a base a wiring substrate with the external electrode electrically connected with said wiring electrode on the top face in the semiconductor chip unit which carries the manufacture approach of the semiconductor device of this invention at least, The process which pastes up two or more semiconductor chips to the top face of said wiring substrate, The process which connects respectively the electrode of said semiconductor chip, and the wiring electrode of said wiring substrate electrically with a metal thin line, The process which closes the enclosure of each semiconductor chip of the top face of said wiring substrate, and a metal thin line by closure resin at least, and forms the closure resin of an abbreviation rectangular

parallelepiped configuration. As opposed to the closure resin side of the cutting field of each semiconductor chip unit on said wiring substrate The process which carries out grinding of said closure resin, deletes it with the 1st broad blade, and makes the periphery of the top face of closure resin a bevel configuration in a cross-section configuration, It is the manufacture approach of a semiconductor device of having the process which cuts said wiring substrate with the 2nd blade with width of face narrower than said 1st blade, divides into each semiconductor chip unit, and obtains a semiconductor device.

[0027] It is the manufacture approach of a semiconductor device of carrying out grinding of said closure resin, deleting it with the 1st broad blade to the closure resin side of the cutting field of each semiconductor chip unit on a wiring substrate, and specifically deleting the closure resin more than 20 of them [%] at the process which makes the periphery of the top face of closure resin a bevel configuration in a cross section configuration when the volume of the closure resin of an abbreviation rectangular parallelepiped configuration is set to 100 [%].

[0028] Moreover, the process which prepares for a wiring electrode and a base a wiring substrate with the external electrode electrically connected with said wiring electrode on the top face in the semiconductor chip unit which carries the manufacture approach of the semiconductor device of this invention at least, The process which pastes up two or more semiconductor chips to the top face of said wiring substrate, The process which connects respectively the electrode of said semiconductor chip, and the wiring electrode of said wiring substrate electrically with a metal thin line, The process which closes the enclosure of each semiconductor chip of the top face of said wiring substrate, and a metal thin line by closure resin at least, It consists of a process which cuts said wiring substrate, divides into each semiconductor chip unit, and obtains a semiconductor device. The process which closes the enclosure of each semiconductor chip of the top face of said wiring substrate, and a metal thin line by closure resin at least It is the manufacture approach of the semiconductor device which is the process which closes where a web material is stuck on the top face other than the field where the metal thin line of said semiconductor chip connected, is exposed from closure resin and closes top faces other than the connection field of the metal thin line of said semiconductor chip.

[0029] It specifically receives in the closure resin side of the cutting field of each semiconductor chip unit on a wiring substrate after the process which closes the enclosure of each semiconductor chip of the top face of said wiring substrate, and a metal thin line by closure resin at least. With the 1st broad blade, carry out grinding of said closure resin, delete it, and it has the process which makes the periphery of the top face of closure resin a bevel configuration in a cross-section configuration. It is the manufacture approach of a semiconductor device of having the process which cuts said wiring substrate with the 2nd blade with width of face narrower than said 1st blade, divides into each semiconductor chip unit, and obtains a semiconductor device next.

[0030] The manufacture approach of the semiconductor device of this invention can manufacture efficiently the semiconductor device of the BGA mold which removed closure resin and realized lightweight-ization using the process of finally separating into the semiconductor device of the piece of an individual by package cutting, using the large-sized substrate in which two or more semiconductor chips can be carried by carrying out grinding of the closure resin with the rotation blade of the shape of a broad-bevel still like a dicing process as said configuration.

[0031]

[Embodiment of the Invention] Hereafter, 1 operation gestalt of the semiconductor device of this invention and its manufacture approach is explained, referring to a drawing.

[0032] The 1st operation gestalt of the semiconductor device of this invention is explained first.

[0033] The semiconductor device of this operation gestalt is a semiconductor device which cut per each semiconductor device and was formed to the wiring substrate to which two or more semiconductor chips were carried in the top face as a basic configuration, and the package closure of the whole surface of the top face was carried out by closure resin.

[0034] Drawing 1, drawing 2, drawing 3, and drawing 4 are drawings showing the semiconductor device of this operation gestalt, and, for drawing 1, a top view and drawing 2 are [the sectional view of one B-B of drawing 1 and drawing 4 of a bottom view and drawing 3] the sectional views of one C-C of drawing 1.

[0035] As shown in drawing 1, drawing 2, drawing 3, and drawing 4, the semiconductor device of this operation gestalt has the external pad electrode which has the wiring electrode 1 on the top face, and was electrically connected to it inside the wiring electrode 1 and substrate on the base (not shown). The semiconductor chip 4 carried on the external pad electrode in the bonding location of the top face of the wiring substrate 3 with the ball electrode 2, and the wiring substrate 3. It consists of a metal thin line 5 which connected electrically the semiconductor chip 4 and the wiring electrode 1 of the wiring substrate 3, and insulating closure resin 6, such as an epoxy resin which closed the top face of the wiring substrate 3.

[0036] When the volume of the closure resin 6 of the abbreviation rectangular parallelepiped configuration of imagination which showed the semiconductor device of this operation gestalt with the broken line as closure resin 6 was deleted, the top-face periphery of closure resin 6 had the oblique side section 10 and it was shown in drawing 3 and drawing 4 is set to 100 [%], the closure resin more than 20 of them [%] is deleted, and the oblique side section 10 is formed here. And thin closure resin 6 remains in the top face of a wiring substrate. With this operation gestalt, when the amount of closure resin is reduced sharply and the volume of the closure resin 6 of the abbreviation rectangular parallelepiped configuration of imagination is set to 100 [%] by carrying out the bevel cut of the top-face periphery of closure resin 6, the closure resin of 35 [%] of them was deleted, weight was reduced by reduction of the amount of closure resin, and the lightweight semiconductor device as a whole is realized.

[0037] That is, in the semiconductor device of this operation gestalt, about the field of the metal thin line 5 which connected the semiconductor chip 4 on the wiring substrate 3, and the wiring electrode 1 and semiconductor chip 4 of the wiring substrate 3, it protected with closure resin 6, the closure resin of parts other than the need was sharply deleted about the closure resin of the top-face part of other wiring substrates 3, and lightweight-ization is realized.

[0038] In the semiconductor device of the BGA mold of a configuration of that the semiconductor device of the BGA mold of this operation gestalt closed the top-face field of the wiring substrate 3 by closure resin While closure resin 6 is deleted, the oblique side section 10 is formed and thin closure resin 6 is remained and formed in the top face of the wiring substrate 3, the top-face periphery of closure resin 6 When the volume of the closure resin of an abbreviation rectangular parallelepiped configuration is set to 100 [%], the closure resin more than 20 of them [%] is deleted, and the oblique side section 10 is formed. Therefore, although the number of the semiconductor chips 4 carried in the wiring substrate 3 with this operation gestalt is one Although the amount of closure resin which closes the top face of a wiring substrate increases when the laminating of the two or more semiconductor chips is carried out and they are carried By adopting the configuration in this operation gestalt, the amount of closure resin can be reduced sharply and lightweight-ization of the weight can be realized also in the semiconductor device of the BGA mold of chip stack structure.

[0039] Of course, since the top-face part of closure resin 6 has the oblique side section 10, the semiconductor device of this operation gestalt can prevent the crack of the closure resin 6 by the impact from the outside, and KAKE. Therefore, it can prevent that the piece of ** into which the closure resin 6 at the time of secondary mounting was broken remains on a mounting substrate, and serves as hindrance of mounting.

[0040] Moreover, in the semiconductor device of this operation gestalt, the ball electrode 2 attached to the wiring substrate 3 is a solder ball, and is attached for the high connection dependability in the case of secondary mounting to a mounting substrate. Moreover, in the arrangement, it is arranged in the shape of a grid to the base of the wiring substrate 3.

[0041] Next, 1 operation gestalt of the manufacture approach of the semiconductor device of the BGA

mold explained with the 1st operation gestalt of this invention is explained. Drawing 5 – drawing 11 are drawings showing the manufacture approach of the semiconductor device of this operation gestalt, and drawing 5 (a) is [a sectional view and drawing 5 (c) of a top view and drawing 5 (b)] bottom views. Moreover, in drawing 6 – drawing 11, it is a top view, (b) is a sectional view, and (a) is considering the part as the top view which penetrated the internal structure in drawing 9 (a).

[0042] The wiring substrate first used with this operation gestalt with reference to drawing 5 is explained.

[0043] As shown in drawing 5, it consists of insulating resin, and a top face is equipped with two or more wiring electrodes 1, and the large-sized wiring substrate 3 equipped with the external pad electrode 8 electrically connected inside the wiring electrode and substrate on the base for semiconductor chip loading is prepared. The external pad electrode 8 is a part to which a ball electrode is attached at a back process. Moreover, the wiring substrate 3 prepared here carries two or more semiconductor chips in one substrate, and prepares the large-sized substrate which can be divided into the semiconductor device of each [after that]. It is break Rhine at the time of the field shown with the broken line being divided into each semiconductor device among drawing 5. Moreover, in drawing 5 (a), the central field surrounded with each wiring electrode 1 constitutes the bonding location in which a semiconductor chip is carried.

[0044] As the manufacture approach of the semiconductor device of this operation gestalt, as first shown in drawing 6, the wiring substrate 3 with the wiring electrode 1 is prepared for a top face as shown in drawing 5.

[0045] And as shown in drawing 7, to each bonding location of the top face of the wiring substrate 3, the top-face side is turned up, adhesion immobilization is carried out with adhesives, and a semiconductor chip 4 is carried respectively. Moreover, flip chip mounting is [as opposed to / loading / a semiconductor chip 4 / substrate / a substrate] sufficient by the arrangement design of a wiring electrode.

[0046] Next, as shown in drawing 8, the electrode pad (not shown) of the semiconductor chip 4 carried on the wiring substrate 3 and the wiring electrode 1 prepared in the top face of the wiring substrate 3 are electrically connected with the metal thin line 5. In addition, since it becomes a connecting means by the bump according to the structure which turned the principal plane up and carried the semiconductor chip 4 in the substrate with this operation gestalt as above-mentioned when flip chip mounting of the semiconductor chip is carried out to a substrate by face down, although the electrical connecting means by the metal thin line 5 is shown, there is no use of a metal thin line.

[0047] And as shown in drawing 9, the whole surface of the top-face field of the wiring substrate 3 is closed with closure resin 6. A transfer mold performs the top-face closure by this closure resin 6, and it closes the substantial whole surface except margin fields, such as a conveyance part of the wiring substrate 3. Moreover, in this phase, an abbreviation rectangular parallelepiped configuration is formed of the closure of the top face of the wiring substrate 3 by closure resin 6. In addition, the broken line shows the condition of having penetrated each configuration of the wiring electrode 1 and a semiconductor chip 4 in drawing 9 (a), and the metal thin line is omitted.

[0048] Next, as shown in drawing 10, to the field of the closure resin 6 of the cutting field of each semiconductor chip 4 unit on the wiring substrate 3, grinding of the closure resin 6 is carried out; it is deleted with the 1st broad rotation blade, the periphery of the top face of closure resin is made into a bevel configuration in a cross-section configuration, and the oblique side section 10 is formed. Here, when the volume of the closure resin 6 of an abbreviation rectangular parallelepiped configuration is set to 100 [%], the closure resin 6 more than 20 of them [%] is deleted, and the closure resin 6 of 35 [%] is deleted with this operation gestalt. Moreover, grinding of the closure resin 6 is carried out in grinding with a rotation blade, and the top face of the wiring substrate 3 is not exposed, and thin closure resin 6 is made to remain in the top face of the wiring substrate 3, and carries out grinding to it. Thereby, top-face protection of the wiring substrate 3 is securable. In addition, about break Rhine of the cutting field

for every semiconductor chip on the field of closure resin 6, a break mark, for example, a marking-off line, and irregularity may be beforehand formed on closure resin 6, and a break field may be recognized with infrared radiation.

[0049] Moreover, to the blade used at the dicing process of the usual semi-conductor wafer being a blade of the width of face of 50 [μm] extent, with this operation gestalt, it is the width of face of 1000 [μm], and the cross-section configuration of a blade uses the bevel blade of a bevel configuration about the 1st broad rotation blade. While carrying out grinding of the closure resin 6 on the wiring substrate 3 and removing it by this, the configuration of the closure resin 6 after grinding is made into a bevel configuration, and the oblique side section 10 can be formed. Moreover, about blade beam, it doubles with spacing of the semiconductor chip and semiconductor chip which were carried on the substrate, and the width of face which can carry out grinding of the top-face periphery of the closure resin of a semiconductor chip located in blade both ends by 1 time of blade grinding is set up.

[0050] Next, as shown in drawing 11, the whole surface closure is carried out by closure resin 6, and in the field of the closure resin 6 of each semiconductor chip 4 unit, to the wiring substrate 3 with which the oblique side section 10 was formed, a top face cuts the wiring substrate 3 with closure resin 6 with the 2nd blade with width of face narrower than the 1st blade used at the last process, and obtains the semiconductor device 11 divided and piece[of an individual]-ized by each semiconductor chip 4 unit. Here, a rotation blade cuts in each semiconductor chip 4 unit along break Rhine for division. It is the same as that of the structure shown in drawing 1, drawing 2, drawing 3, and drawing 4 as structure of the semiconductor device 11 obtained here, and closure resin is deleted, the top-face periphery of the closure resin 6 of a semiconductor device 11 has the oblique side section 10, and thin closure resin 6 remains in the circumference top face of the wiring substrate 3. And when the volume of the closure resin of an abbreviation rectangular parallelepiped configuration is set to 100 [%], the closure resin 6 more than 20 of them [%] is deleted, and the oblique side section is formed.

[0051] Moreover, in the case of cutting with a rotation blade, a piece of individual-like semiconductor device can be obtained with a sufficient precision by cutting along break Rhine for division established in the wiring substrate 3. Usually, the dicing facility used by the semi-conductor production process performs division with this rotation blade. Moreover, although it may cut from the case [where it cuts from the base side of a substrate], and closure resin 6 side on the top face of a substrate in case division cutting is carried out at the piece of an individual, with this operation gestalt, it is cutting from the base side of the wiring substrate 3. Thereby, a wiring substrate can be cut in the condition of having held to stability.

[0052] To each piece[of an individual]-ized semiconductor device, a solder ball is attached to the external pad electrode of the base of the wiring substrate 3 as a back process, the ball electrode 2 is formed, and an external terminal is constituted. Or before forming the semiconductor device which cut and piece[of an individual]-ized the wiring substrate, a ball electrode can be efficiently formed to the whole wiring substrate by forming a ball electrode per one substrate on the external pad electrode of the base of a wiring substrate.

[0053] The manufacture approach of the semiconductor device of this operation gestalt can manufacture efficiently the semiconductor device of the BGA mold which carried out grinding removal of the amount of closure resin with the broad rotation blade like the dicing process, and realized lightweight-ization using the process of finally separating into the semiconductor device of the piece of an individual by package cutting, using the large-sized substrate in which two or more semiconductor chips can be carried as mentioned above.

[0054] Next, the 2nd operation gestalt of the semiconductor device of this invention is explained.

[0055] The semiconductor device of this operation gestalt is a semiconductor device which cut per each semiconductor device and was formed to the wiring substrate to which two or more semiconductor chips were carried in the top face as a basic configuration, and the package closure of the whole surface of the top face was carried out by closure resin.

[0056] Drawing 12, drawing 13, drawing 14, and drawing 15 are drawings showing the semiconductor device of this operation gestalt, and, for drawing 12, a top view and drawing 13 are [the sectional view of one D-D of drawing 12 and drawing 15 of a bottom view and drawing 14] the sectional views of one E-E of drawing 12.

[0057] As shown in drawing 12, drawing 13, drawing 14, and drawing 15, the semiconductor device of this operation gestalt The wiring substrate 3 with the external pad electrode (not shown) electrically connected with the wiring electrode on the wiring electrode 1 and the base on the top face, The metal thin line 5 which connected the semiconductor chip 4 with which the base was carried in the wiring substrate 3 by pasting up, and the electrode of the semiconductor chip 4 and the wiring electrode 1 of the wiring substrate 3, It consists of closure resin 6 which closed some semiconductor chips 4 of the top face of the wiring substrate 3, and the field of the metal thin line 5. Top faces other than the connection field of the metal thin line 5 of a semiconductor chip 4 are semiconductor devices exposed from closure resin 6, and the ball electrode 2 is attached on the external pad electrode of the base of the wiring substrate 3, and they constitute the external terminal. And some closure resin is deleted and the top-face periphery of closure resin 6 has the oblique side section 10. Moreover, thin closure resin 6 remains in the top-face periphery of the wiring substrate 3.

[0058] When the volume of the closure resin 6 of the abbreviation rectangular parallelepiped configuration of imagination which showed the semiconductor device of this operation gestalt with the broken line as closure resin 6 was deleted, the top-face periphery of closure resin 6 had the oblique side section 10 and it was shown in drawing 14 and drawing 15 is set to 100 [%], the closure resin more than 20 of them [%] is deleted, and the oblique side section 10 is formed here. When the volume of the closure resin 6 of the abbreviation rectangular parallelepiped configuration of imagination is furthermore set to 100 [%], the top face of a semiconductor chip 4 is exposed by removing the closure resin more than 20 of them [%]. This has deleted the closure resin more than 40 [%] of the whole. And thin closure resin 6 remains in the top face of a wiring substrate. The closure resin of top faces other than the connection field of the metal thin line 5 of a semiconductor chip 4 and the closure resin of the top-face periphery of closure resin are deleted by this, the amount of closure resin more than 40 [%] is reduced, and-izing can be carried out [lightweight] as a semiconductor device.

[0059] That is, in the semiconductor device of this operation gestalt, about the field of the metal thin line 5 which connected the semiconductor chip 4 on the wiring substrate 3, and the wiring electrode 1 and semiconductor chip 4 of the wiring substrate 3, it protected with closure resin 6, the closure resin of parts other than the need was sharply deleted about the closure resin of other semiconductor chip 4 top faces or the top-face part of the wiring substrate 3, and lightweight-ization is realized.

[0060] While reducing the amount of closure resin sharply by carrying out the bevel cut of the top-face periphery of closure resin 6 with this operation gestalt It is made to expose except for the closure resin of fields other than the metal thin line field of the top face of a semiconductor chip 4. When the volume of the closure resin 6 of the abbreviation rectangular parallelepiped configuration of imagination is set to 100 [%], the closure resin of 55 [%] of them was deleted, weight was reduced by reduction of the amount of closure resin, and the semiconductor device of a lightweight BGA mold as a whole is realized.

[0061] Although the amount of closure resin which closes the top face of a wiring substrate increases when the laminating of the two or more semiconductor chips is carried out and they are carried, although the number of the semiconductor chips 4 carried in the wiring substrate 3 with this operation gestalt is one, by adopting the configuration in this operation gestalt, the amount of closure resin can be reduced sharply and lightweight-ization of the weight can be realized also in the semiconductor device of the BGA mold-of chip stack structure.

[0062] Of course, since the top-face part of closure resin 6 has the oblique side section 10, the semiconductor device of this operation gestalt can prevent the crack of the closure resin 6 by the impact from the outside, and KAKE. Therefore, it can prevent that the piece of ** into which the closure resin 6 at the time of secondary mounting was broken remains on a mounting substrate, and serves as

hindrance of mounting.

[0063] Moreover, in the semiconductor device of this operation gestalt, the ball electrode 2 attached to the wiring substrate 3 is a solder ball, and is attached for the high connection dependability in the case of secondary mounting to a mounting substrate. Moreover, in the arrangement, it is arranged in the shape of a grid to the base of the wiring substrate 3.

[0064] Next, 1 operation gestalt of the manufacture approach of the semiconductor device of the BGA mold explained with the 2nd operation gestalt of this invention is explained. Drawing 16 – drawing 22 are drawings showing the manufacture approach of the semiconductor device of this operation gestalt, and drawing 16 (a) is [a sectional view and drawing 16 (c) of a top view and drawing 16 (b)] bottom views. Moreover, in drawing 17 – drawing 22, it is a top view, (b) is a sectional view, and (a) is considering the part as the top view which penetrated the internal structure in drawing 20 (a).

[0065] The wiring substrate first used with this operation gestalt with reference to drawing 16 is explained.

[0066] As shown in drawing 16, it consists of insulating resin, and a top face is equipped with two or more wiring electrodes 1, and the large-sized wiring substrate 3 equipped with the external pad electrode 8 electrically connected inside the wiring electrode and substrate on the base for semiconductor chip loading is prepared. The external pad electrode 8 is a part to which a ball electrode is attached at a back process. Moreover, the wiring substrate 3 prepared here carries two or more semiconductor chips in one substrate, and prepares the large-sized substrate which can be divided into the semiconductor device of each [after that]. It is break Rhine at the time of the field shown with the broken line being divided into each semiconductor device among drawing 16. Moreover, in drawing 16 (a), the central field surrounded with each wiring electrode 1 constitutes the bonding location in which a semiconductor chip is carried.

[0067] As the manufacture approach of the semiconductor device of this operation gestalt, as first shown in drawing 17, the wiring substrate 3 with the wiring electrode 1 is prepared for a top face as shown in drawing 16.

[0068] And as shown in drawing 18, to each bonding location of the top face of the wiring substrate 3, the top-face side is turned up, adhesion immobilization is carried out with adhesives, and a semiconductor chip 4 is carried respectively. Moreover, flip chip mounting is [as opposed to / loading / a semiconductor chip 4 / substrate / a substrate] sufficient by the arrangement design of a wiring electrode.

[0069] Next, as shown in drawing 19, the electrode pad (not shown) of the semiconductor chip 4 carried on the wiring substrate 3 and the wiring electrode 1 prepared in the top face of the wiring substrate 3 are electrically connected with the metal thin line 5. In addition, since it becomes a connecting means by the bump according to the structure which turned the principal plane up and carried the semiconductor chip 4 in the substrate with this operation gestalt as above-mentioned when flip chip mounting of the semiconductor chip is carried out to a substrate by face down, although the electrical connecting means by the metal thin line 5 is shown, there is no use of a metal thin line.

[0070] And as shown in drawing 20, package closure of the enclosure of each semiconductor chip 4 of the top face of the wiring substrate 3 and the metal thin line 5 is carried out by closure resin 6 at least. At this process, where the field which should perform the selection closure, and should be made to stick a web material to top faces other than the field where the metal thin line 5 of a semiconductor chip 4 connected, and a semiconductor chip 4 should expose with closure metal mold with a protection feature is covered, it closes. By the resin seal by closure metal mold with this web material and a protection feature, it can be made to be able to expose from closure resin 6, and top faces other than the connection field of the metal thin line 5 of a semiconductor chip 4 can be closed. By exposure from the closure resin 6 of this semiconductor chip 4, the closure resin of 20 [%] can be deleted to the amount of closures of original closure resin.

[0071] Moreover, a transfer mold performs the top-face closure by this closure resin 6, and it closes the

substantial whole surface except margin fields, such as a conveyance part of the wiring substrate 3. Moreover, in this phase, an abbreviation rectangular parallelepiped configuration is formed except for a semiconductor chip exposure of the closure of the top face of the wiring substrate 3 by closure resin 6. In addition, the broken line shows the condition of having penetrated each configuration of the wiring electrode 1 and a semiconductor chip 4 in drawing 20 (a), and the metal thin line is omitted.

[0072] Next, as shown in drawing 21, to the field of the closure resin 6 of the cutting field of each semiconductor chip 4 unit on the wiring substrate 3, grinding of the closure resin 6 is carried out, it is deleted with the 1st broad rotation blade, the periphery of the top face of closure resin is made into a bevel configuration in a cross-section configuration, and the oblique side section 10 is formed. Here, when the volume of the closure resin 6 of an abbreviation rectangular parallelepiped configuration is set to 100 [%], the closure resin 6 more than 20 of them [%] is deleted, and the closure resin 6 of 35 [%] is deleted with this operation gestalt. Moreover, grinding of the closure resin 6 is carried out in grinding with a rotation blade, and the top face of the wiring substrate 3 is not exposed, and thin closure resin 6 is made to remain in the top face of the wiring substrate 3, and carries out grinding to it. Thereby, top-face protection of the wiring substrate 3 is securable. In addition, about break Rhine of the cutting field for every semiconductor chip on the field of closure resin 6, a break mark, for example, a marking-off line, and irregularity may be beforehand formed on closure resin 6, and a break field may be recognized with infrared radiation.

[0073] Moreover, to the blade used at the dicing process of the usual semi-conductor wafer being a blade of the width of face of 50 [μm] extent, with this operation gestalt, it is the width of face of 1000 [μm], and the cross-section configuration of a blade uses the bevel blade of a bevel configuration about the 1st broad rotation blade. While carrying out grinding of the closure resin 6 on the wiring substrate 3 and removing it by this, the configuration of the closure resin 6 after grinding is made into a bevel configuration, and the oblique side section 10 can be formed. Moreover, about blade beam, it doubles with spacing of the semiconductor chip and semiconductor chip which were carried on the substrate, and the width of face which can carry out grinding of the top-face periphery of the closure resin of a semiconductor chip located in blade both ends by 1 time of blade grinding is set up.

[0074] Next, as shown in drawing 22, top faces other than the field connected with the metal thin line 5 of a semiconductor chip 4 are exposed, the whole surface closure of the other top face is carried out by closure resin 6, and it sets to the field of the closure resin 6 of each semiconductor chip 4 unit. The wiring substrate 3 is cut with closure resin 6 to the wiring substrate 3 with which the oblique side section 10 was formed with the 2nd blade with width of face narrower than the 1st blade used at the last process, and the semiconductor device 12 divided and piece[of an individual]-ized by each semiconductor chip 4 unit is obtained. Here, a rotation blade cuts in each semiconductor chip 4 unit along break Rhine for division. It is the same as that of the structure shown in drawing 12, drawing 13, drawing 14, and drawing 15 as structure of the semiconductor device 12 obtained here, and a part of top face of the semiconductor chip 4 of a semiconductor device 12 is exposed from closure resin 6, and closure resin 6 is deleted, the top-face periphery of closure resin 6 has the oblique side section 10, and thin closure resin 6 remains in the circumference top face of the wiring substrate 3. And when the volume of the closure resin of an abbreviation rectangular parallelepiped configuration is set to 100 [%], the closure resin of 20 [%] of them is removed, the top face of a semiconductor chip 4 is exposed, the closure resin 6 more than further 20 [%] is deleted, the oblique side section 10 is formed, it is total, and the closure resin 6 more than 40 [%] was deleted, and lightweight-ization is realized.

[0075] Moreover, in the case of cutting with a rotation blade, a piece of individual-like semiconductor device can be obtained with a sufficient precision by cutting along break Rhine for division established in the wiring substrate 3. Usually, the dicing facility used by the semi-conductor production process performs division with this rotation blade. Moreover, although it may cut from the case [where it cuts from the base side of a substrate], and closure resin 6 side on the top face of a substrate in case division cutting is carried out at the piece of an individual, with this operation gestalt, it is cutting from

the base side of the wiring substrate 3. Thereby, a wiring substrate can be cut in the condition of having held to stability.

[0076] To each piece[of an individual]-ized semiconductor device, a solder ball is attached to the external pad electrode of the base of the wiring substrate 3 as a back process, the ball electrode 2 is formed, and an external terminal is constituted. Or before forming the semiconductor device which cut and piece[of an individual]-ized the wiring substrate, a ball electrode can be efficiently formed to the whole wiring substrate by forming a ball electrode per one substrate on the external pad electrode of the base of a wiring substrate.

[0077] The manufacture approach of the semiconductor device of this operation gestalt can manufacture efficiently the semiconductor device of the BGA mold which reduced the amount of closure resin and realized lightweight-ization using the process of finally separating into the semiconductor device of the piece of an individual by package cutting, using the large-sized substrate in which two or more semiconductor chips can be carried as mentioned above.

[0078] As mentioned above, since it corresponds to small lightweight-ization of the electronic equipment requested from ***** in the semiconductor device of a BGA mold as each operation gestalt of this invention explained, the amount of the closure resin which constitutes the semiconductor device can be reduced, and the whole can be lightweight-ized. With this operation gestalt, in each configuration, such as electric connecting means, such as a wiring substrate which constitutes the semiconductor device, a semiconductor chip, and a metal thin line, closure resin, and a ball electrode, even if it deletes the amount of closure resin efficiently uninfluential on dependability as a semiconductor device, and the laminating of two or more semiconductor chips is carried out, they are carried in a wiring substrate paying attention to the closure resin which can contribute to lightweight-ization greatly and increase of closure resin starts, lightweight-ization can be attained.

[0079]

[Effect of the Invention] As mentioned above, when closure resin is deleted, the top-face periphery of closure resin has the oblique side section and the volume of the closure resin of the abbreviation rectangular parallelepiped configuration of imagination is set to 100 [%], the closure resin more than 20 of them [%] is deleted, and the semiconductor device of this invention forms the oblique side section, as the operation gestalt explained. Therefore, weight is reduced by reduction of the amount of closure resin, and a lightweight semiconductor device as a whole can be realized.

[0080] Moreover, the manufacture approach of the semiconductor device of this invention develops a dicing process, can carry out grinding removal of the closure resin with a rotation blade, and can manufacture efficiently the semiconductor device of the BGA mold which reduced the amount of closure resin and realized lightweight-ization while it utilizes the efficient manufacture method of construction using the process of finally separating into the semiconductor device of the piece of an individual by package blade cutting, using the large-sized substrate in which two or more semiconductor chips can be carried.

[Translation done.]

* NOTICES *

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.

2. **** shows the word which can not be translated.

3. In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The top view showing the semiconductor device of 1 operation gestalt of this invention

[Drawing 2] The bottom view showing the semiconductor device of 1 operation gestalt of this invention

[Drawing 3] The sectional view showing the semiconductor device of 1 operation gestalt of this invention

[Drawing 4] The sectional view showing the semiconductor device of 1 operation gestalt of this invention

[Drawing 5] Drawing showing the manufacture approach of the semiconductor device of 1 operation gestalt of this invention

[Drawing 6] Drawing showing the manufacture approach of the semiconductor device of 1 operation gestalt of this invention

[Drawing 7] Drawing showing the manufacture approach of the semiconductor device of 1 operation gestalt of this invention

[Drawing 8] Drawing showing the manufacture approach of the semiconductor device of 1 operation gestalt of this invention

[Drawing 9] Drawing showing the manufacture approach of the semiconductor device of 1 operation gestalt of this invention

[Drawing 10] Drawing showing the manufacture approach of the semiconductor device of 1 operation gestalt of this invention

[Drawing 11] Drawing showing the manufacture approach of the semiconductor device of 1 operation gestalt of this invention

[Drawing 12] The top view showing the semiconductor device of 1 operation gestalt of this invention

[Drawing 13] The bottom view showing the semiconductor device of 1 operation gestalt of this invention

[Drawing 14] The sectional view showing the semiconductor device of 1 operation gestalt of this invention

[Drawing 15] The sectional view showing the semiconductor device of 1 operation gestalt of this invention

[Drawing 16] Drawing showing the manufacture approach of the semiconductor device of 1 operation gestalt of this invention

[Drawing 17] Drawing showing the manufacture approach of the semiconductor device of 1 operation gestalt of this invention

[Drawing 18] Drawing showing the manufacture approach of the semiconductor device of 1 operation gestalt of this invention

[Drawing 19] Drawing showing the manufacture approach of the semiconductor device of 1 operation gestalt of this invention

[Drawing 20] Drawing showing the manufacture approach of the semiconductor device of 1 operation gestalt of this invention

[Drawing 21] Drawing showing the manufacture approach of the semiconductor device of 1 operation gestalt of this invention

[Drawing 22] Drawing showing the manufacture approach of the semiconductor device of 1 operation gestalt of this invention

[Drawing 23] The top view showing the conventional semiconductor device

[Drawing 24] The bottom view showing the conventional semiconductor device

[Drawing 25] The sectional view showing the conventional semiconductor device

[Drawing 26] The sectional view showing the conventional semiconductor device

[Drawing 27] Drawing showing the manufacture approach of the conventional semiconductor device

[Drawing 28] The top view showing the manufacture approach of the conventional semiconductor device

[Drawing 29] The top view showing the manufacture approach of the conventional semiconductor device

[Drawing 30] The top view showing the manufacture approach of the conventional semiconductor device

[Description of Notations]

1 Wiring Electrode

2 Ball Electrode

3 Wiring Substrate

4 Semiconductor Chip

5 Metal Thin Line

6 Closure Resin

7 Oblique Side Section

8 External Pad Electrode

9 Semiconductor Device

10 Oblique Side Section

11 Semiconductor Device

12 Semiconductor Device

[Translation done.]

(19)日本国特許庁 (JP)

(12) 公開特許公報 (A)

(11)特許出願公開番号
特開2002-134661
(P2002-134661A)

(43)公開日 平成14年5月10日 (2002.5.10)

(51)Int.Cl.
H 01 L 23/28
21/56
23/12

識別記号
501

F I
H 01 L 23/28
21/56
23/12

テマコード(参考)
J 4 M 1 0 9
R 5 F 0 6 1
5 0 1 W
5 0 1 B

審査請求 未請求 請求項の数11 OL (全 16 頁)

(21)出願番号 特願2000-326602(P2000-326602)
(22)出願日 平成12年10月26日 (2000.10.26)

(71)出願人 000005821
松下電器産業株式会社
大阪府門真市大字門真1006番地
(72)発明者 藤本 博昭
大阪府高槻市幸町1番1号 松下電子工業
株式会社内
(72)発明者 佐原 隆一
大阪府高槻市幸町1番1号 松下電子工業
株式会社内
(74)代理人 100097445
弁理士 岩橋 文雄 (外2名)

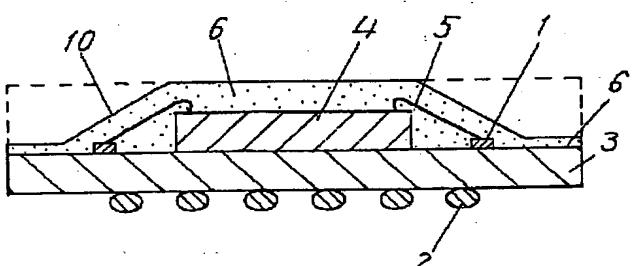
最終頁に続く

(54)【発明の名称】 半導体装置およびその製造方法

(57)【要約】

【課題】 電子機器の小型軽量化の要望にしたがい、BGA型の半導体装置においてもその軽量化が問題となっていた。

【解決手段】 上面に配線電極1を有し、底面にボール電極2を有した配線基板3と、配線基板3の上面に搭載された半導体チップ4と、半導体チップ4と配線基板3の配線電極1とを接続した金属細線5と、配線基板3の上面を封止した絶縁性の封止樹脂6により構成され、封止樹脂6の上面周辺部は封止樹脂6が削除されて斜辺部10を有しており、仮想の略直方体形状の封止樹脂6の体積を100[%]とした場合、その内の2.0[%]以上の封止樹脂が削除されている。これにより上面周辺部の封止樹脂量を大幅に削減し、重量を低減させ、全体として軽量なBGA型の半導体装置を実現している。



(2)

【特許請求の範囲】

【請求項 1】 上面に配線電極と底面に前記配線電極と電気的に接続した外部電極を有した配線基板と、前記配線基板にその底面が接着されて搭載された半導体チップと、前記半導体チップの電極と前記配線基板の配線電極とを接続した金属細線と、前記配線基板の上面を封止した封止樹脂によりなり、前記封止樹脂の上面周辺部は封止樹脂が削除されて斜辺を有していることを特徴とする半導体装置。

【請求項 2】 封止樹脂の上面周辺部は封止樹脂が削除されて斜辺を有し、配線基板の上面には薄厚の封止樹脂が残存していることを特徴とする請求項 1 に記載の半導体装置。

【請求項 3】 略直方体形状の封止樹脂の体積を 100 [%] とした場合、その内の 20 [%] 以上の封止樹脂が削除されて斜辺を有していることを特徴とする請求項 1 に記載の半導体装置。

【請求項 4】 上面に配線電極と底面に前記配線電極と電気的に接続した外部電極を有した配線基板と、前記配線基板にその底面が接着されて搭載された半導体チップと、前記半導体チップの電極と前記配線基板の配線電極とを接続した金属細線と、前記配線基板の上面の前記半導体チップの一部、金属細線の領域を封止した封止樹脂によりなり、前記半導体チップの金属細線の接続領域以外の上面は封止樹脂から露出されていることを特徴とする半導体装置。

【請求項 5】 封止樹脂の上面周辺部は封止樹脂が削除されて斜辺を有していることを特徴とする請求項 4 に記載の半導体装置。

【請求項 6】 封止樹脂の上面周辺部は封止樹脂が削除されて斜辺を有し、配線基板の上面には薄厚の封止樹脂が残存していることを特徴とする請求項 4 に記載の半導体装置。

【請求項 7】 略直方体形状の封止樹脂の体積を 100 [%] とした場合、その内の 40 [%] 以上の封止樹脂が削除されていることを特徴とする請求項 4 に記載の半導体装置。

【請求項 8】 少なくとも搭載する半導体チップ単位でその上面に配線電極と底面に前記配線電極と電気的に接続した外部電極を有した配線基板を用意する工程と、前記配線基板の上面に対して、複数の半導体チップを接着する工程と、前記半導体チップの電極と前記配線基板の配線電極とを各々金属細線により電気的に接続する工程と、少なくとも前記配線基板の上面の各半導体チップ、金属細線の外囲を封止樹脂で封止する工程と、前記配線基板を切断し、各半導体チップ単位に分割して半導体装置を得る工程とよりなり、前記半導体チップの金属細線の接続領域以外の上面は封止樹脂から露出されていることを特徴とする半導体装置。

2

前記配線基板上の各半導体チップ単位の切断領域の封止樹脂面に対して、幅広の第 1 のブレードで前記封止樹脂を研削して削除し、封止樹脂の上面の周辺部を断面形状でペベル形状にする工程と、

前記第 1 のブレードよりも幅の狭い第 2 のブレードで前記配線基板を切断し、各半導体チップ単位に分割して半導体装置を得る工程とを有することを特徴とする半導体装置の製造方法。

【請求項 9】 配線基板上の各半導体チップ単位の切断領域の封止樹脂面に対して、幅広の第 1 のブレードで前記封止樹脂を研削して削除し、封止樹脂の上面の周辺部を断面形状でペベル形状にする工程では、略直方体形状の封止樹脂の体積を 100 [%] とした場合、その内の 20 [%] 以上の封止樹脂を削除することを特徴とする請求項 8 に記載の半導体装置の製造方法。

【請求項 10】 少なくとも搭載する半導体チップ単位でその上面に配線電極と底面に前記配線電極と電気的に接続した外部電極を有した配線基板を用意する工程と、前記配線基板の上面に対して、複数の半導体チップを接着する工程と、

前記半導体チップの電極と前記配線基板の配線電極とを各々金属細線により電気的に接続する工程と、少なくとも前記配線基板の上面の各半導体チップ、金属細線の外囲を封止樹脂で封止する工程と、前記配線基板を切断し、各半導体チップ単位に分割して半導体装置を得る工程とよりなり、

少なくとも前記配線基板の上面の各半導体チップ、金属細線の外囲を封止樹脂で封止する工程は、シート材を前記半導体チップの金属細線が接続された領域以外の上面に密着させた状態で封止し、前記半導体チップの金属細線の接続領域以外の上面を封止樹脂から露出させて封止する工程であることを特徴とする半導体装置の製造方法。

【請求項 11】 少なくとも前記配線基板の上面の各半導体チップ、金属細線の外囲を封止樹脂で封止する工程の後に、配線基板上の各半導体チップ単位の切断領域の封止樹脂面に対して、幅広の第 1 のブレードで前記封止樹脂を研削して削除し、封止樹脂の上面の周辺部を断面形状でペベル形状にする工程を有し、この後に、前記第 1 のブレードよりも幅の狭い第 2 のブレードで前記配線基板を切断し、各半導体チップ単位に分割して半導体装置を得る工程とを有することを特徴とする請求項 10 に記載の半導体装置の製造方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】 本発明は半導体チップが搭載された基板の上面が封止樹脂で封止され、基板底面にボール電極が付設されたボールグリッドアレイ (BGA) タイプの半導体装置およびその製造方法に関するものであり、特に電子機器の小型軽量化に対応できる軽量化を

(3)

3

実現した半導体装置およびその製造方法に関するものである。

【0002】

【従来の技術】エリアアレイタイプの半導体装置として、半導体チップが搭載された基板の上面が封止樹脂で封止され、基板底面にボール電極が付設されたBGAタイプの半導体装置がある。

【0003】以下、従来の半導体装置について図面を参照しながら説明する。図23、図24、図25は従来の半導体装置として、BGA型の半導体装置を示す図であり、図23は平面図、図24は底面図、図25は図23のA-A1箇所の断面図である。

【0004】図23、図24および図25に示すように従来の半導体装置は、上面に配線電極1を有し、底面にその配線電極1と基板内部で電気的に接続した外部パッド電極（図示せず）と、その外部パッド電極上にボール電極2を有した配線基板3と、配線基板3の上面のボンディング位置に搭載された半導体チップ4と、半導体チップ4と配線基板3の配線電極1とを電気的に接続した金属細線5と、配線基板3の上面を封止した絶縁性の封止樹脂6により構成されたものである。従来の半導体装置において外形形状としては、各側面は垂直な面を有し、全体として矩形状をなしているものである。なおこの外形形状は製造過程上の形状である。

【0005】また従来の半導体装置において、配線基板3に付設されたボール電極2は半田ボールであり、実装基板への二次実装の際の高接続信頼性のために付設されている。またその配置においては配線基板3の底面に対して格子状に配置されているものである。

【0006】また従来の半導体装置の別形態としては、図26の断面図に示すように、二次実装時の信頼性を考慮して、配線基板3の上面を封止した封止樹脂6の上面の周辺部に斜辺部7を形成し、角部を削除したBGA型の半導体装置もある。

【0007】次に従来の半導体装置の製造方法について説明する。図27～図30は従来の半導体装置の製造方法を示す図であり、図27(a)は平面図、図27(b)は底面図であり、図28～図30は平面図である。また図29、図30においては一部、内部構造を透過した平面図としている。

【0008】まず図27(a)、(b)に示すように、絶縁性樹脂より構成され、搭載する半導体チップ単位で上面に複数の配線電極1を備え、底面にその配線電極1と基板内部で電気的に接続した外部パッド電極8を備えた半導体チップ搭載用の大型の配線基板3を用意する。外部パッド電極8は後工程でボール電極が付設される部分である。またここで用意する配線基板3は、1枚の基板に複数の半導体チップを搭載し、その後で個々の半導体装置に分割するための大型の基板を用意するものである。図27中、破線で示した領域が個々の半導体装置に

4

分割される際の区切りラインである。また図27(a)において、各配線電極1で包囲された中央領域が半導体チップを搭載するボンディング位置を構成するものである。

【0009】次に図28(a)に示すように、図27に示したような配線基板3を用意し、図28(b)に示すように、配線基板3の上面の各ボンディング位置に対し各々、半導体チップ4を接着剤により接着固定して搭載する。

【0010】次に図29(a)に示すように、配線基板3上に搭載した半導体チップ4の電極パッド（図示せず）と配線基板3の上面に設けられた配線電極1とを金属細線5により電気的に接続する。

【0011】そして図29(b)に示すように、配線基板3の上面全面を封止樹脂6により封止する。この封止樹脂6による上面封止はトランスマーモールドにより行う。なお図29(b)においては配線電極1、半導体チップ4の各構成を透過した状態を破線で示しており、金属細線は省略している。

【0012】そして図30に示すように、上面が封止樹脂6で全面封止された配線基板3に対して、回転ブレードにより各半導体チップ4の単位ごとに切断することにより、個片化された半導体装置9を得るものである。ここで得られた半導体装置9の構造としては図23、図24、図25に示した構造と同一であるため図示は省略する。

【0013】ここで回転ブレードによる切断の際は、配線基板3に設けた分割用の区切りラインに沿って切断することにより、精度よく個片状の半導体装置を得ることができる。通常、この回転ブレードによる分割は、半導体製造工程で用いられる20 [μm] 程度の幅のブレードを用いたダイシング設備によって行うものである。また個片に分割切断する際、配線基板3の底面側から切断する場合と、基板上面の封止樹脂6側から切断する場合がある。

【0014】個片化した各半導体装置に対しては、後工程として配線基板3の底面の外部パッド電極に半田ボールを付設してボール電極を形成し、外部端子を構成する。

【0015】以上のように従来は、複数個の半導体チップを搭載可能な大型の基板を用いて、その基板に半導体チップを搭載、電気的な接続、樹脂封止を行い、最終に一括切断で個片に分離するという工程によりBGA型の半導体装置を製造していた。

【0016】

【発明が解決しようとする課題】しかしながら前記従来の半導体装置およびその製造方法では、複数個の半導体チップを搭載可能な大型の基板を用いて、その基板に半導体チップを搭載し、電気的な接続後、樹脂封止を行い、最後に個片にブレード切断するという工程によりB

(4)

5

G A型の半導体装置を製造していたため、その製造上の特徴として、得られた半導体装置の外形形状が各側面が垂直な面を有し、全体として矩形状をなしているものであった。そのため半導体装置としては封止樹脂の体積量が多く、全体重量の軽量化は達成できなかった。また従来の半導体装置として、半導体装置の封止樹脂の上面周辺部の各角部を削除した構造があるが、この角部削除の目的は、半導体装置を実装基板への実装する（二次実装）際の角部の割れ、カケを防止する目的であり、封止樹脂の削減量としては5 [%] 程度の範囲であり、軽量化に寄与できるほどのものではなかった。

【0017】本発明は製造効率の低下を招くことなく半導体装置を製造するとともに、実装基板等への二次実装時の信頼性を高め、さらに封止樹脂の重量に着目して半導体装置として大幅に軽量化を達成できる半導体装置およびその製造方法を提供することを目的とする。特に近将来において配線基板上に複数の半導体チップが積層搭載されたスタック構造のB G A型の半導体装置において懸念される封止樹脂の重量を削減し、電子機器の小型軽量化に対応できる軽量化を実現する半導体装置およびその製造方法を提供することを目的とする。

【0018】

【課題を解決するための手段】前記従来の課題を解決するために本発明の半導体装置は、上面に配線電極と底面に前記配線電極と電気的に接続した外部電極を有した配線基板と、前記配線基板にその底面が接着されて搭載された半導体チップと、前記半導体チップの電極と前記配線基板の配線電極とを接続した金属細線と、前記配線基板の上面を封止した封止樹脂とよりなり、前記封止樹脂の上面周辺部は封止樹脂が削除されて斜辺を有している半導体装置である。

【0019】具体的には、封止樹脂の上面周辺部は封止樹脂が削除されて斜辺を有し、配線基板の上面には薄厚の封止樹脂が残存している半導体装置である。

【0020】また、略直方体形状の封止樹脂の体積を100 [%]とした場合、その内の20 [%]以上の封止樹脂が削除されて斜辺を有している半導体装置である。

【0021】また本発明の半導体装置は、上面に配線電極と底面に前記配線電極と電気的に接続した外部電極を有した配線基板と、前記配線基板にその底面が接着されて搭載された半導体チップと、前記半導体チップの電極と前記配線基板の配線電極とを接続した金属細線と、前記配線基板の上面の前記半導体チップの一部、金属細線の領域を封止した封止樹脂とよりなり、前記半導体チップの金属細線の接続領域以外の上面は封止樹脂から露出されている半導体装置である。

【0022】具体的には、封止樹脂の上面周辺部は封止樹脂が削除されて斜辺を有している半導体装置である。

【0023】また、封止樹脂の上面周辺部は封止樹脂が削除されて斜辺を有し、配線基板の上面には薄厚の封止

6

樹脂が残存している半導体装置である。

【0024】また、略直方体形状の封止樹脂の体積を100 [%]とした場合、その内の40 [%]以上の封止樹脂が削除されている半導体装置である。

【0025】前記構成の通り本発明の半導体装置は、封止樹脂の上面周辺部をベベルカットすることにより斜辺部を構成し、大幅に封止樹脂量を削減し、仮想の略直方体形状の封止樹脂の体積を100 [%]とした場合、その内の20 [%]以上の封止樹脂を削除し、封止樹脂量の削減により重量を低減させ、全体として軽量な半導体装置を実現できるものである。

【0026】本発明の半導体装置の製造方法は、少なくとも搭載する半導体チップ単位でその上面に配線電極と底面に前記配線電極と電気的に接続した外部電極を有した配線基板を用意する工程と、前記配線基板の上面に対して、複数の半導体チップを接着する工程と、前記半導体チップの電極と前記配線基板の配線電極とを各々金属細線により電気的に接続する工程と、少なくとも前記配線基板の上面の各半導体チップ、金属細線の外囲を封止樹脂で封止して略直方体形状の封止樹脂を形成する工程と、前記配線基板上の各半導体チップ単位の切断領域の封止樹脂面に対して、幅広の第1のブレードで前記封止樹脂を研削して削除し、封止樹脂の上面の周辺部を断面形状でベベル形状にする工程と、前記第1のブレードよりも幅の狭い第2のブレードで前記配線基板を切断し、各半導体チップ単位に分割して半導体装置を得る工程とを有する半導体装置の製造方法である。

【0027】具体的には、配線基板上の各半導体チップ単位の切断領域の封止樹脂面に対して、幅広の第1のブレードで前記封止樹脂を研削して削除し、封止樹脂の上面の周辺部を断面形状でベベル形状にする工程では、略直方体形状の封止樹脂の体積を100 [%]とした場合、その内の20 [%]以上の封止樹脂を削除する半導体装置の製造方法である。

【0028】また本発明の半導体装置の製造方法は、少なくとも搭載する半導体チップ単位でその上面に配線電極と底面に前記配線電極と電気的に接続した外部電極を有した配線基板を用意する工程と、前記配線基板の上面に対して、複数の半導体チップを接着する工程と、前記半導体チップの電極と前記配線基板の配線電極とを各々金属細線により電気的に接続する工程と、少なくとも前記配線基板の上面の各半導体チップ、金属細線の外囲を封止樹脂で封止する工程と、前記配線基板を切断し、各半導体チップ単位に分割して半導体装置を得る工程となり、少なくとも前記配線基板の上面の各半導体チップ、金属細線の外囲を封止樹脂で封止する工程は、シート材を前記半導体チップの金属細線が接続された領域以外の上面に密着させた状態で封止し、前記半導体チップの金属細線の接続領域以外の上面を封止樹脂から露出させて封止する工程である半導体装置の製造方法である。

【0029】具体的には、少なくとも前記配線基板の上面の各半導体チップ、金属細線の外囲を封止樹脂で封止する工程の後に、配線基板上の各半導体チップ単位の切断領域の封止樹脂面に対して、幅広の第1のブレードで前記封止樹脂を研削して削除し、封止樹脂の上面の周辺部を断面形状でペベル形状にする工程を有し、この後に、前記第1のブレードよりも幅の狭い第2のブレードで前記配線基板を切断し、各半導体チップ単位に分割して半導体装置を得る工程とを有する半導体装置の製造方法である。

【0030】前記構成の通り本発明の半導体装置の製造方法は、複数個の半導体チップを搭載可能な大型の基板を用いて、最終的に一括切断で個片の半導体装置に分離するという工程を用い、さらにダイシング工程と同様に幅広のペベル状の回転ブレードで封止樹脂を研削することにより、封止樹脂を除去して軽量化を実現したBGA型の半導体装置を効率よく製造できるものである。

【0031】

【発明の実施の形態】以下、本発明の半導体装置およびその製造方法の一実施形態について、図面を参照しながら説明する。

【0032】まず本発明の半導体装置の第1の実施形態について説明する。

【0033】本実施形態の半導体装置は基本構成として、その上面に複数の半導体チップが搭載され、その上面の全面が封止樹脂で一括封止された配線基板に対して、個々の半導体装置単位に切断して形成された半導体装置である。

【0034】図1、図2、図3および図4は本実施形態の半導体装置を示す図であり、図1は平面図、図2は底面図、図3は図1のB-B1箇所の断面図、図4は図1のC-C1箇所の断面図である。

【0035】図1、図2、図3および図4に示すように、本実施形態の半導体装置は、上面に配線電極1を有し、底面にその配線電極1と基板内部で電気的に接続した外部パット電極（図示せず）と、その外部パット電極上にポール電極2を有した配線基板3と、配線基板3の上面のボンディング位置に搭載された半導体チップ4と、半導体チップ4と配線基板3の配線電極1とを電気的に接続した金属細線5と、配線基板3の上面を封止したエポキシ樹脂等の絶縁性の封止樹脂6とより構成されたものである。

【0036】ここで本実施形態の半導体装置は、封止樹脂6の上面周辺部は封止樹脂6が削除されて斜辺部10を有しており、図3、図4に示すように、破線で示した仮想の略直方体形状の封止樹脂6の体積を100[%]とした場合、その内の20[%]以上の封止樹脂が削除されて斜辺部10を形成している。そして配線基板の上面には薄厚の封止樹脂6が残存しているものである。本実施形態では封止樹脂6の上面周辺部をペベルカットす

ることにより大幅に封止樹脂量を削減し、仮想の略直方体形状の封止樹脂6の体積を100[%]とした場合、その内の35[%]の封止樹脂を削除し、封止樹脂量の削減により重量を低減させ、全体として軽量な半導体装置を実現している。

【0037】すなわち本実施形態の半導体装置では、配線基板3上の半導体チップ4、および配線基板3の配線電極1と半導体チップ4とを接続した金属細線5の領域については封止樹脂6により保護し、他の配線基板3の上面部分の封止樹脂については必要以外の部分の封止樹脂を大幅に削除して軽量化を実現しているものである。

【0038】本実施形態のBGA型の半導体装置は、配線基板3の上面領域を封止樹脂で封止した構成のBGA型の半導体装置において、封止樹脂6の上面周辺部は封止樹脂6が削除されて斜辺部10が形成され、配線基板3の上面には薄厚の封止樹脂6が残存して形成されるとともに、略直方体形状の封止樹脂の体積を100[%]とした場合、その内の20[%]以上の封止樹脂が削除されて斜辺部10を形成しているものである。したがって、本実施形態では配線基板3に搭載する半導体チップ4は1つであるが、2つ以上の半導体チップを積層して搭載した場合には、配線基板の上面を封止する封止樹脂量は増大するが、本実施形態での構成を採用することにより、大幅に封止樹脂の量を削減でき、チップスタック構造のBGA型の半導体装置においてもその重量の軽量化を実現できるものである。

【0039】もちろん本実施形態の半導体装置は、封止樹脂6の上面部分は斜辺部10を有しているので、外部からの衝撃による封止樹脂6の割れ、カケを防止できるものである。したがって二次実装時の封止樹脂6の割れた欠片が実装基板上に残存して実装の妨げとなることを防止できる。

【0040】また本実施形態の半導体装置において、配線基板3に付設されたポール電極2は半田ボールであり、実装基板への二次実装の際の高接続信頼性のために付設されている。またその配置においては配線基板3の底面に対して格子状に配置されているものである。

【0041】次に本発明の第1の実施形態で説明したBGA型の半導体装置の製造方法の一実施形態について説明する。図5～図11は本実施形態の半導体装置の製造方法を示す図であり、図5(a)は平面図、図5(b)は断面図、図5(c)は底面図である。また図6～図11において、(a)は平面図、(b)は断面図であり、図9(a)においては一部、内部構造を透過した平面図としている。

【0042】まず図5を参照して本実施形態で用いる配線基板について説明する。

【0043】図5に示すように、絶縁性樹脂より構成され、上面に複数の配線電極1を備え、底面にその配線電極と基板内部で電気的に接続した外部パット電極8を備

(6)

9

えた大型の半導体チップ搭載用の配線基板3を用意する。外部パッド電極8は後工程でポール電極が付設される部分である。またここで用意する配線基板3は、1枚の基板に複数の半導体チップを搭載し、その後で個々の半導体装置に分割することができる大型の基板を用意するものである。図5中、破線で示した領域が個々の半導体装置に分割される際の区切りラインである。また図5(a)において、各配線電極1で包囲された中央領域が半導体チップを搭載するボンディング位置を構成するものである。

【0044】本実施形態の半導体装置の製造方法としては、まず図6に示すように、図5に示したような上面に配線電極1を有した配線基板3を用意する。

【0045】そして図7に示すように、配線基板3の上面の各ボンディング位置に対して各々、半導体チップ4をその上面側を上にして接着剤により接着固定して搭載する。また半導体チップ4の基板搭載については、配線電極の配置設計により基板に対してフリップチップ実装でもよい。

【0046】次に図8に示すように、配線基板3上に搭載した半導体チップ4の電極パッド(図示せず)と配線基板3の上面に設けられた配線電極1とを金属細線5により電気的に接続する。なお本実施形態では前述の通り、半導体チップ4をその正面を上にして基板に搭載した構造により、金属細線5による電気的接続手段を示しているが、半導体チップをフェースダウンにより基板に対してフリップチップ実装した場合はバンプによる接続手段となるため金属細線の使用はない。

【0047】そして図9に示すように、配線基板3の上面領域の全面を封止樹脂6により封止する。この封止樹脂6による上面封止はトランシスファーモールドにより行うもので、配線基板3の搬送部分等のマージン領域を除いた実質的な全面を封止するものである。またこの段階では、封止樹脂6による配線基板3の上面の封止により、略直方体形状が形成されるものである。なお図9(a)においては配線電極1、半導体チップ4の各構成を透過した状態を破線で示しており、金属細線は省略している。

【0048】次に図10に示すように、配線基板3上の各半導体チップ4単位の切断領域の封止樹脂6の面に対して、幅広の第1の回転ブレードで封止樹脂6を研削して削除し、封止樹脂の上面の周辺部を断面形状でベベル形状にし、斜辺部10を形成する。ここでは略直方体形状の封止樹脂6の体積を100[%]とした場合、その内の20[%]以上の封止樹脂6を削除するものであり、本実施形態では35[%]の封止樹脂6を削除している。また回転ブレードによる研削においては封止樹脂6を研削して配線基板3の上面を露出させるものではなく、配線基板3の上面には薄厚の封止樹脂6を残存させて研削するものである。これにより配線基板3の上面保

10

護は確保できる。なお、封止樹脂6の面上の半導体チップごとの切断領域の区切りラインについては、区切り目印、例えばけがき線や凹凸を封止樹脂6上に予め形成しておいてもよいし、赤外線で区切り領域を認識してもよい。

【0049】また幅広の第1の回転ブレードについては、通常の半導体ウェハーのダイシング工程で用いているブレードは50[μm]程度の幅のブレードであるのに対して、本実施形態では1000[μm]の幅であって、ブレードの断面形状がベベル形状のベベルブレードを用いている。これにより配線基板3上の封止樹脂6を研削して除去するとともに、研削後の封止樹脂6の形状をベベル形状とし、斜辺部10を形成できるものである。またブレード幅については、基板上に搭載された半導体チップと半導体チップとの間隔に合わせ、1回のブレード研削でブレード両端に位置する半導体チップの封止樹脂の上面周辺部を研削できる幅を設定する。

【0050】次に図11に示すように、上面が封止樹脂6で全面封止され、各半導体チップ4単位の封止樹脂6の領域において、斜辺部10が形成された配線基板3に対して、前工程で用いた第1のブレードよりも幅の狭い第2のブレードで配線基板3を封止樹脂6とともに切断し、各半導体チップ4単位に分割して個片化された半導体装置11を得る。ここでは回転ブレードにより分割用の区切りラインに沿って各半導体チップ4単位に切断するものである。ここで得られた半導体装置11の構造としては図1、図2、図3、図4に示した構造と同一であり、半導体装置11の封止樹脂6の上面周辺部は封止樹脂が削除されて斜辺部10を有し、配線基板3の周辺上面には薄厚の封止樹脂6が残存しているものである。そして略直方体形状の封止樹脂の体積を100[%]とした場合、その内の20[%]以上の封止樹脂6が削除されて斜辺部を形成しているものである。

【0051】また回転ブレードによる切断の際は、配線基板3に設けた分割用の区切りラインに沿って切断することにより、精度よく個片状の半導体装置を得ることができる。通常、この回転ブレードによる分割は、半導体製造工程で用いられるダイシング設備によって行うものである。また個片に分割切断する際、基板の底面側から切断する場合と、基板上面の封止樹脂6側から切断する場合とがあるが、本実施形態では配線基板3の底面側から切断している。これにより配線基板を安定に保持した状態で切断できる。

【0052】個片化した各半導体装置に対しては、後工程として配線基板3の底面の外部パッド電極に半田ボールを付設してポール電極2を形成し、外部端子を構成する。または配線基板を切断して個片化した半導体装置を形成する前に、配線基板全体に対して、配線基板の底面の外部パッド電極上にポール電極を1枚の基板単位で形成することにより効率よくポール電極を形成できる。

(7)

11

【0053】以上のように本実施形態の半導体装置の製造方法は、複数個の半導体チップを搭載可能な大型の基板を用いて、最終的に一括切断で個片の半導体装置に分離するという工程を用い、ダイシング工程と同様に幅広の回転ブレードで封止樹脂の量を研削除去して軽量化を実現したBGA型の半導体装置を効率よく製造できるものである。

【0054】次に本発明の半導体装置の第2の実施形態について説明する。

【0055】本実施形態の半導体装置は基本構成として、その上面に複数の半導体チップが搭載され、その上面の全面が封止樹脂で一括封止された配線基板に対して、個々の半導体装置単位に切断して形成された半導体装置である。

【0056】図12、図13、図14および図15は本実施形態の半導体装置を示す図であり、図12は平面図、図13は底面図、図14は図12のD-D1箇所の断面図、図15は図12のE-E1箇所の断面図である。

【0057】図12、図13、図14および図15に示すように、本実施形態の半導体装置は、上面に配線電極1と底面に配線電極と電気的に接続した外部パッド電極(図示せず)を有した配線基板3と、その配線基板3に底面が接着されて搭載された半導体チップ4と、その半導体チップ4の電極と配線基板3の配線電極1とを接続した金属細線5と、配線基板3の上面の半導体チップ4の一部、金属細線5の領域を封止した封止樹脂6によりなり、半導体チップ4の金属細線5の接続領域以外の上面は封止樹脂6から露出されている半導体装置であり、配線基板3の底面の外部パッド電極上にはボール電極2が付設されて外部端子を構成している。そして封止樹脂6の上面周辺部は封止樹脂の一部が削除されて斜辺部10を有しているものである。また配線基板3の上面周辺部には薄厚の封止樹脂6が残存しているものである。

【0058】ここで本実施形態の半導体装置は、封止樹脂6の上面周辺部は封止樹脂6が削除されて斜辺部10を有しており、図14、図15に示すように、破線で示した仮想の略直方体形状の封止樹脂6の体積を100[%]とした場合、その内の20[%]以上の封止樹脂が削除されて斜辺部10を形成している。さらに仮想の略直方体形状の封止樹脂6の体積を100[%]とした場合、その内の20[%]以上の封止樹脂を除くことにより半導体チップ4の上面を露出させている。これにより全体の40[%]以上の封止樹脂を削除しているものである。

そして配線基板の上面には薄厚の封止樹脂6が残存しているものである。これにより半導体チップ4の金属細線5の接続領域以外の上面の封止樹脂と、封止樹脂の上面周辺部の封止樹脂とが削除され、40[%]以上の封止樹脂量を低減させ、半導体装置として軽量化できるものである。

12

【0059】すなわち本実施形態の半導体装置では、配線基板3上の半導体チップ4、および配線基板3の配線電極1と半導体チップ4とを接続した金属細線5の領域については封止樹脂6により保護し、他の半導体チップ4上面や配線基板3の上面部分の封止樹脂については必要以外の部分の封止樹脂を大幅に削除して軽量化を実現しているものである。

【0060】本実施形態では封止樹脂6の上面周辺部をペベルカットすることにより大幅に封止樹脂量を削減するとともに、半導体チップ4の上面の金属細線領域以外の領域の封止樹脂を除いて露出させ、仮想の略直方体形状の封止樹脂6の体積を100[%]とした場合、その内の55[%]の封止樹脂を削除し、封止樹脂量の削減により重量を低減させ、全体として軽量なBGA型の半導体装置を実現している。

【0061】本実施形態では配線基板3に搭載する半導体チップ4は1つであるが、2つ以上の半導体チップを積層して搭載した場合には、配線基板の上面を封止する封止樹脂量は増大するが、本実施形態での構成を採用することにより、大幅に封止樹脂の量を削減でき、チップスタック構造のBGA型の半導体装置においてもその重量の軽量化を実現できるものである。

【0062】もちろん本実施形態の半導体装置は、封止樹脂6の上面部分は斜辺部10を有しているので、外部からの衝撃による封止樹脂6の割れ、カケを防止できるものである。したがって二次実装時の封止樹脂6の割れた欠片が実装基板上に残存して実装の妨げとなることを防止できる。

【0063】また本実施形態の半導体装置において、配線基板3に付設されたボール電極2は半田ボールであり、実装基板への二次実装の際の高接続信頼性のために付設されている。またその配置においては配線基板3の底面に対して格子状に配置されているものである。

【0064】次に本発明の第2の実施形態で説明したBGA型の半導体装置の製造方法の一実施形態について説明する。図16～図22は本実施形態の半導体装置の製造方法を示す図であり、図16(a)は平面図、図16(b)は断面図、図16(c)は底面図である。また図17～図22において、(a)は平面図、(b)は断面図であり、図20(a)においては一部、内部構造を透過した平面図としている。

【0065】まず図16を参照して本実施形態で用いる配線基板について説明する。

【0066】図16に示すように、絶縁性樹脂より構成され、上面に複数の配線電極1を備え、底面にその配線電極と基板内部で電気的に接続した外部パッド電極8を備えた大型の半導体チップ搭載用の配線基板3を用意する。外部パッド電極8は後工程でボール電極が付設される部分である。またここで用意する配線基板3は、1枚の基板に複数の半導体チップを搭載し、その後で個々の

(8)

13

半導体装置に分割することができる大型の基板を用意するものである。図16中、破線で示した領域が個々の半導体装置に分割される際の区切りラインである。また図16(a)において、各配線電極1で包囲された中央領域が半導体チップを搭載するボンディング位置を構成するものである。

【0067】本実施形態の半導体装置の製造方法としては、まず図17に示すように、図16に示したような上面に配線電極1を有した配線基板3を用意する。

【0068】そして図18に示すように、配線基板3の上面の各ボンディング位置に対して各々、半導体チップ4をその上面側を上にして接着剤により接着固定して搭載する。また半導体チップ4の基板搭載については、配線電極の配置設計により基板に対してフリップチップ実装でもよい。

【0069】次に図19に示すように、配線基板3上に搭載した半導体チップ4の電極パッド(図示せず)と配線基板3の上面に設けられた配線電極1とを金属細線5により電気的に接続する。なお本実施形態では前述の通り、半導体チップ4をその正面を上にして基板に搭載した構造により、金属細線5による電気的接続手段を示しているが、半導体チップをフェースダウンにより基板に対してフリップチップ実装した場合はバンプによる接続手段となるため金属細線の使用はない。

【0070】そして図20に示すように、少なくとも配線基板3の上面の各半導体チップ4、金属細線5の外周を封止樹脂6で一括封止する。この工程では選択封止を行い、シート材を半導体チップ4の金属細線5が接続された領域以外の上面に密着させ、かつ保護機能を有した封止金型で半導体チップ4の露出させるべき面をカバーした状態で封止する。このシート材、保護機能を有した封止金型による樹脂封止で、半導体チップ4の金属細線5の接続領域以外の上面を封止樹脂6から露出させて封止することができる。この半導体チップ4の封止樹脂6からの露出により、本来の封止樹脂の封止量に対して20[%]の封止樹脂を削除できる。

【0071】またこの封止樹脂6による上面封止はトランസファーモールドにより行うもので、配線基板3の搬送部分等のマージン領域を除いた実質的な全面を封止するものである。またこの段階では、封止樹脂6による配線基板3の上面の封止により、半導体チップ露出面を除いて略直方体形状が形成されるものである。なお図20(a)においては配線電極1、半導体チップ4の各構成を透過した状態を破線で示しており、金属細線は省略している。

【0072】次に図21に示すように、配線基板3上の各半導体チップ4単位の切断領域の封止樹脂6の面に対して、幅広の第1の回転ブレードで封止樹脂6を研削して削除し、封止樹脂の上面の周辺部を断面形状でベベル形状にし、斜辺部10を形成する。ここでは略直方体形

14

状の封止樹脂6の体積を100[%]とした場合、その内の20[%]以上の封止樹脂6を削除するものであり、本実施形態では35[%]の封止樹脂6を削除している。また回転ブレードによる研削においては封止樹脂6を研削して配線基板3の上面を露出させるものではなく、配線基板3の上面には薄厚の封止樹脂6を残存させて研削するものである。これにより配線基板3の上面保護は確保できる。なお、封止樹脂6の面上の半導体チップごとの切断領域の区切りラインについては、区切り目印、例えはげき線や凹凸を封止樹脂6上に予め形成しておいてもよいし、赤外線で区切り領域を認識してもよい。

【0073】また幅広の第1の回転ブレードについては、通常の半導体ウェハーのダイシング工程で用いているブレードは50[μm]程度の幅のブレードであるのに対して、本実施形態では1000[μm]の幅であって、ブレードの断面形状がベベル形状のベベルブレードを用いている。これにより配線基板3上の封止樹脂6を研削して除去するとともに、研削後の封止樹脂6の形状をベベル形状とし、斜辺部10を形成できるものである。またブレード幅については、基板上に搭載された半導体チップと半導体チップとの間隔に合わせ、1回のブレード研削でブレード両端に位置する半導体チップの封止樹脂の上面周辺部を研削できる幅を設定する。

【0074】次に図22に示すように、半導体チップ4の金属細線5で接続された領域以外の上面が露出され、それ以外の上面が封止樹脂6で全面封止され、各半導体チップ4単位の封止樹脂6の領域において、斜辺部10が形成された配線基板3に対して、前工程で用いた第1のブレードよりも幅の狭い第2のブレードで配線基板3を封止樹脂6とともに切断し、各半導体チップ4単位に分割して個片化された半導体装置12を得る。ここでは回転ブレードにより分割用の区切りラインに沿って各半導体チップ4単位に切断するものである。ここで得られた半導体装置12の構造としては図12、図13、図14、図15に示した構造と同一であり、半導体装置12の半導体チップ4の上面の一部は封止樹脂6から露出し、また封止樹脂6の上面周辺部は封止樹脂6が削除されて斜辺部10を有し、配線基板3の周辺上面には薄厚の封止樹脂6が残存しているものである。そして略直方体形状の封止樹脂の体積を100[%]とした場合、その内の20[%]の封止樹脂が除去されて半導体チップ4の上面が露出し、さらに20[%]以上の封止樹脂6が削除されて斜辺部10を形成しているものであり、トータルで40[%]以上の封止樹脂6が削除されて軽量化を実現しているものである。

【0075】また回転ブレードによる切断の際は、配線基板3に設けた分割用の区切りラインに沿って切断することにより、精度よく個片状の半導体装置を得ることができる。通常、この回転ブレードによる分割は、半導体

(9)

15

製造工程で用いられるダイシング設備によって行うものである。また個片に分割切断する際、基板の底面側から切断する場合と、基板上面の封止樹脂6側から切断する場合とがあるが、本実施形態では配線基板3の底面側から切断している。これにより配線基板を安定に保持した状態で切断できる。

【0076】個片化した各半導体装置に対しては、後工程として配線基板3の底面の外部パッド電極に半田ボールを付設してボール電極2を形成し、外部端子を構成する。または配線基板を切断して個片化した半導体装置を形成する前に、配線基板全体に対して、配線基板の底面の外部パッド電極上にボール電極を1枚の基板単位で形成することにより効率よくボール電極を形成できる。

【0077】以上のように本実施形態の半導体装置の製造方法は、複数個の半導体チップを搭載可能な大型の基板を用いて、最終的に一括切断で個片の半導体装置に分離するという工程を用い、封止樹脂の量を削減して軽量化を実現したBGA型の半導体装置を効率よく製造できるものである。

【0078】以上、本発明の各実施形態で説明した通り、BGA型の半導体装置において、近将来に要望される電子機器の小型軽量化に対応するために、半導体装置を構成している封止樹脂の量を低減し、全体を軽量化することができる。本実施形態では、半導体装置を構成している配線基板、半導体チップ、金属細線等の電気的な接続手段、封止樹脂、ボール電極などの各構成において、軽量化に大きく貢献できる封止樹脂に着目し、半導体装置として信頼性上に影響なく、効率よく封止樹脂の量を削除し、半導体チップが複数個、積層されて配線基板に搭載され、封止樹脂の増大がおこっても、軽量化を達成できるものである。

【0079】

【発明の効果】以上、実施形態で説明した通り、本発明の半導体装置は、封止樹脂の上面周辺部は封止樹脂が削除されて斜辺部を有しており、仮想の略直方体形状の封止樹脂の体積を100[%]とした場合、その内の20[%]以上の封止樹脂が削除されて斜辺部を形成している。そのため、封止樹脂量の削減により重量を低減させ、全体として軽量な半導体装置を実現できるものである。

【0080】また本発明の半導体装置の製造方法は、複数個の半導体チップを搭載可能な大型の基板を用いて、最終的に一括ブレード切断で個片の半導体装置に分離するという工程を用いた効率的な製造工法を活用するとともに、ダイシング工程を発展させて回転ブレードで封止樹脂を研削除去でき、封止樹脂の量を削減して軽量化を実現したBGA型の半導体装置を効率よく製造できるものである。

【図面の簡単な説明】

【図1】本発明の一実施形態の半導体装置を示す平面図

16

【図2】本発明の一実施形態の半導体装置を示す底面図
【図3】本発明の一実施形態の半導体装置を示す断面図
【図4】本発明の一実施形態の半導体装置を示す断面図
【図5】本発明の一実施形態の半導体装置の製造方法を示す図

【図6】本発明の一実施形態の半導体装置の製造方法を示す図

【図7】本発明の一実施形態の半導体装置の製造方法を示す図

【図8】本発明の一実施形態の半導体装置の製造方法を示す図

【図9】本発明の一実施形態の半導体装置の製造方法を示す図

【図10】本発明の一実施形態の半導体装置の製造方法を示す図

【図11】本発明の一実施形態の半導体装置の製造方法を示す図

【図12】本発明の一実施形態の半導体装置を示す平面図

【図13】本発明の一実施形態の半導体装置を示す底面図

【図14】本発明の一実施形態の半導体装置を示す断面図

【図15】本発明の一実施形態の半導体装置を示す断面図

【図16】本発明の一実施形態の半導体装置の製造方法を示す図

【図17】本発明の一実施形態の半導体装置の製造方法を示す図

【図18】本発明の一実施形態の半導体装置の製造方法を示す図

【図19】本発明の一実施形態の半導体装置の製造方法を示す図

【図20】本発明の一実施形態の半導体装置の製造方法を示す図

【図21】本発明の一実施形態の半導体装置の製造方法を示す図

【図22】本発明の一実施形態の半導体装置の製造方法を示す図

【図23】従来の半導体装置を示す平面図

【図24】従来の半導体装置を示す底面図

【図25】従来の半導体装置を示す断面図

【図26】従来の半導体装置を示す断面図

【図27】従来の半導体装置の製造方法を示す図

【図28】従来の半導体装置の製造方法を示す平面図

【図29】従来の半導体装置の製造方法を示す平面図

【図30】従来の半導体装置の製造方法を示す平面図

【符号の説明】

1. 配線電極

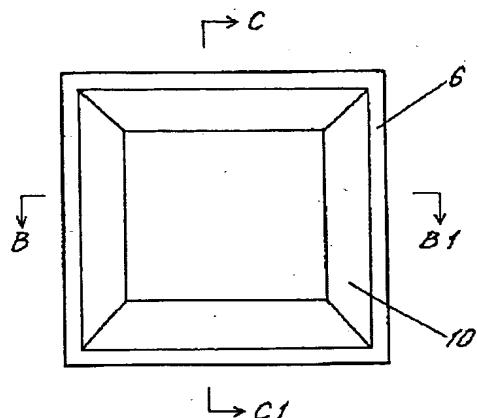
2. ボール電極

(10)

17

3 配線基板
4 半導体チップ
5 金属細線
6 封止樹脂
7 斜辺部

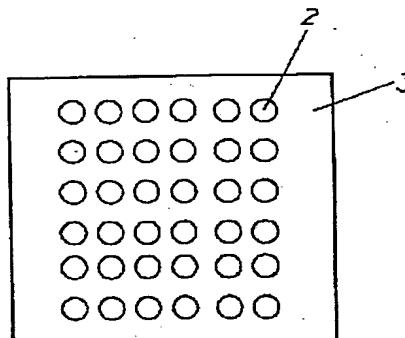
【図1】



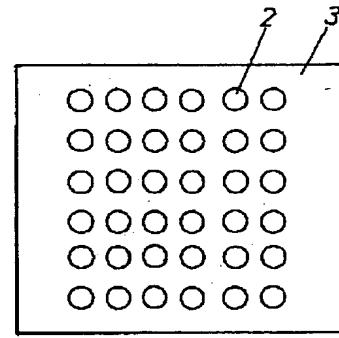
18

8 外部パッド電極
9 半導体装置
10 斜辺部
11 半導体装置
12 半導体装置

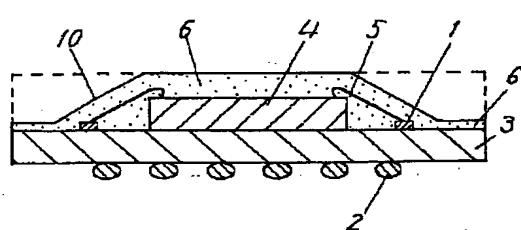
【図2】



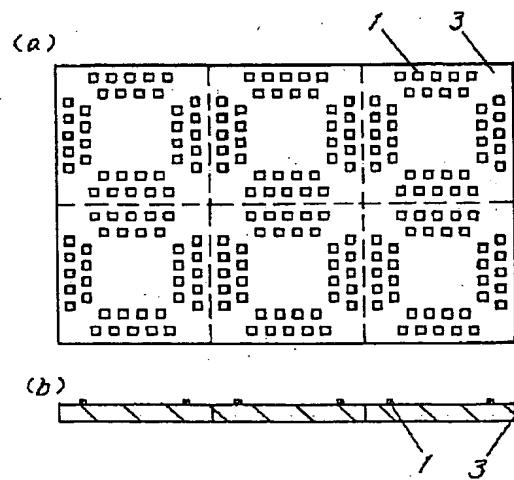
【図13】



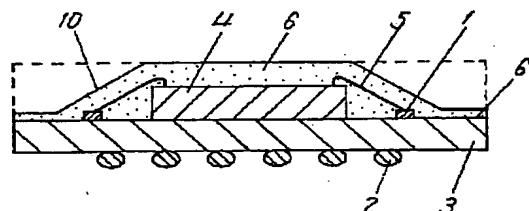
【図3】



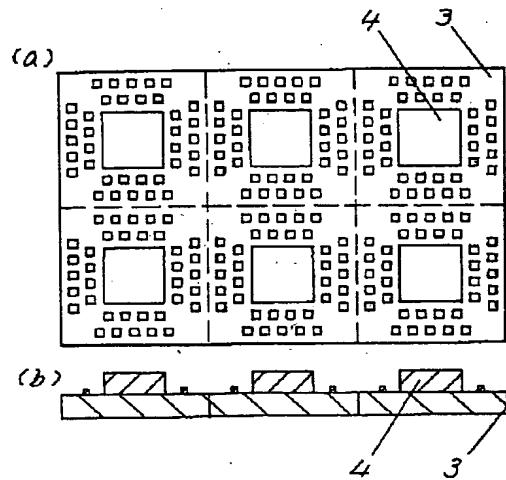
【図6】



【図4】

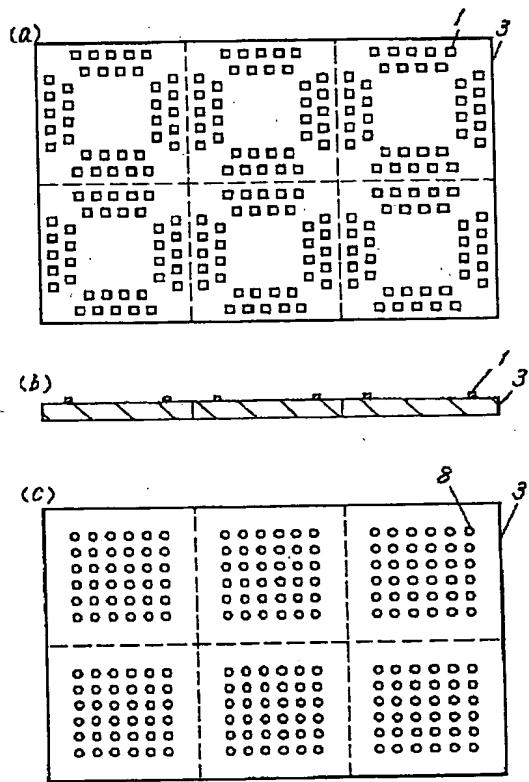


【図7】

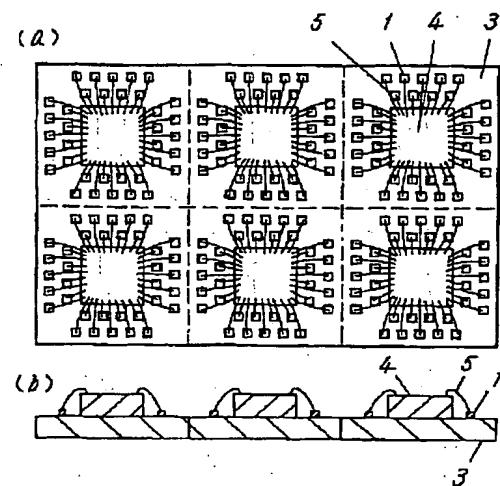


(11)

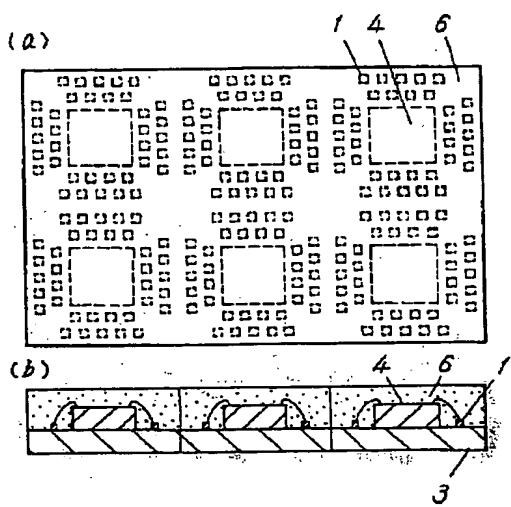
【図5】



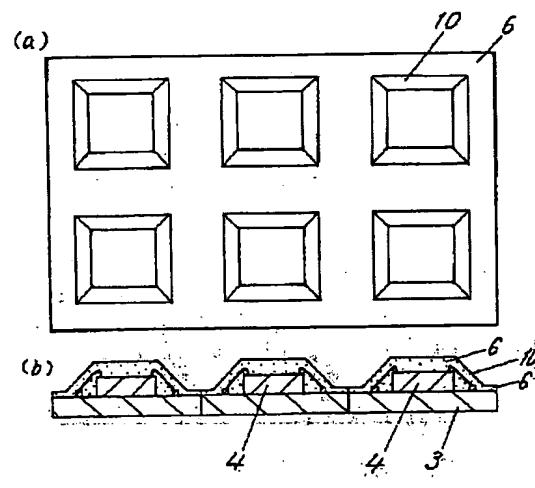
【図8】



【図9】

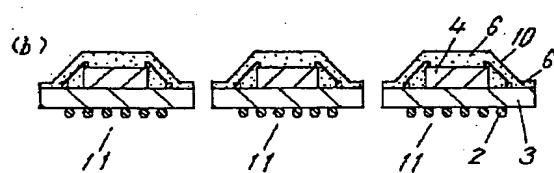
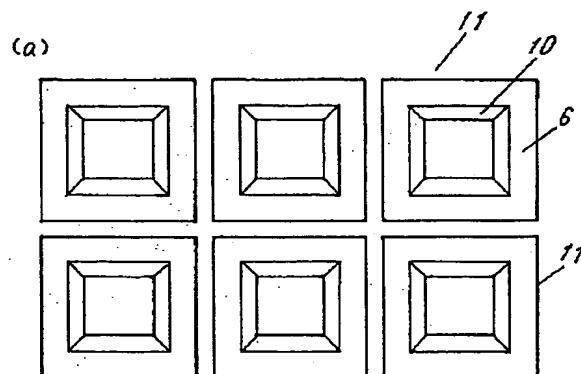


【図10】

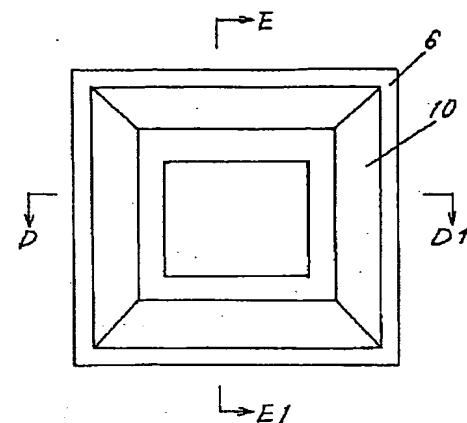


(12)

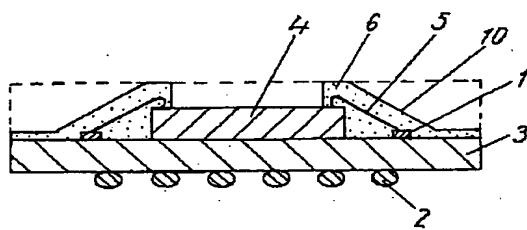
【図11】



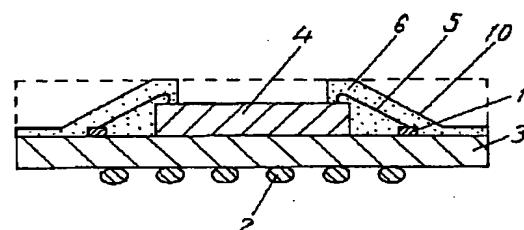
【図12】



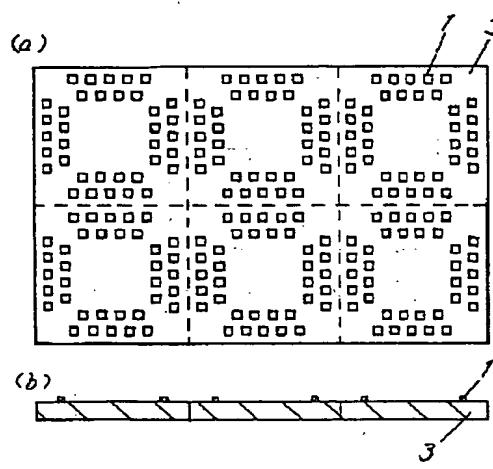
【図14】



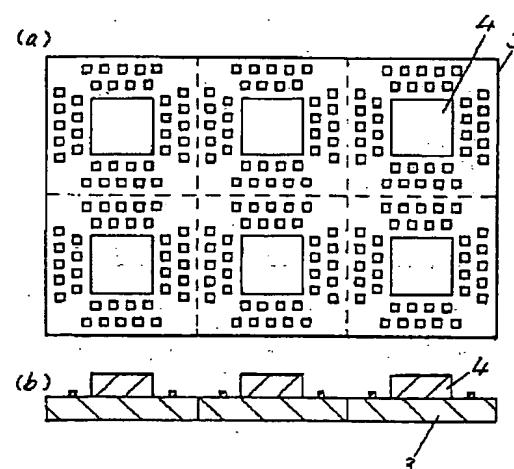
【図15】



【図17】

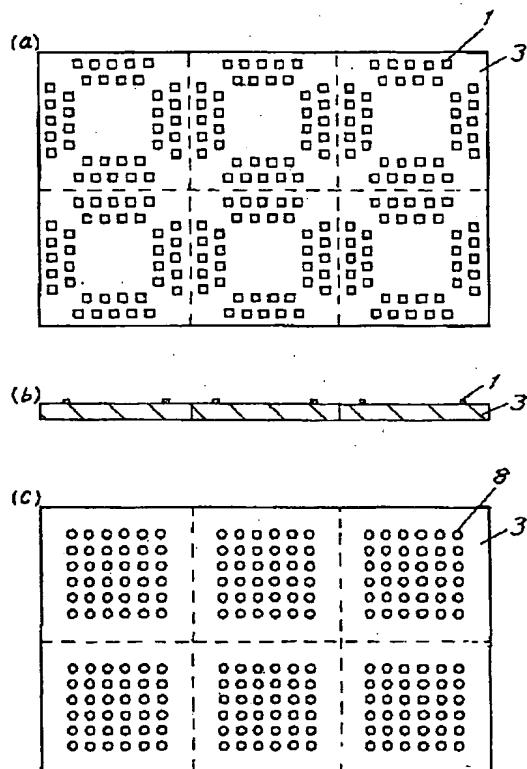


【図18】

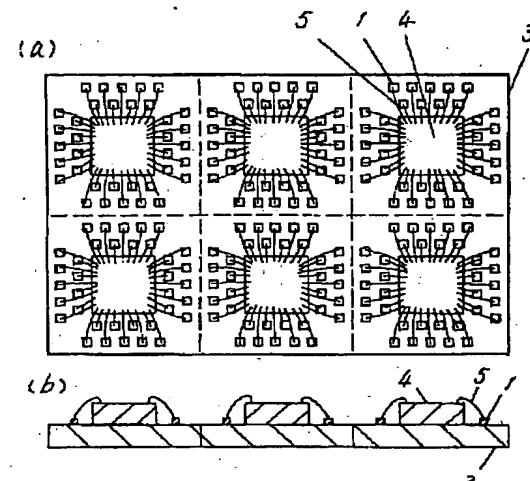


(13)

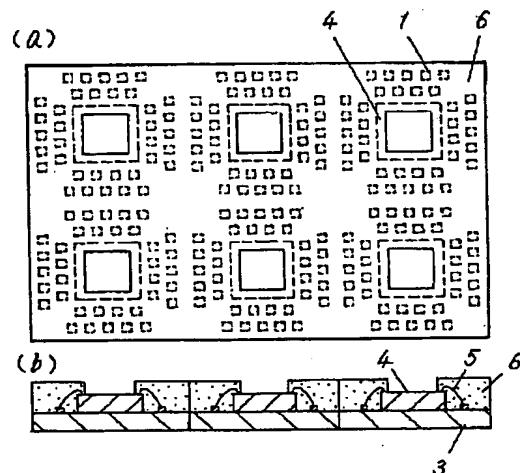
【図16】



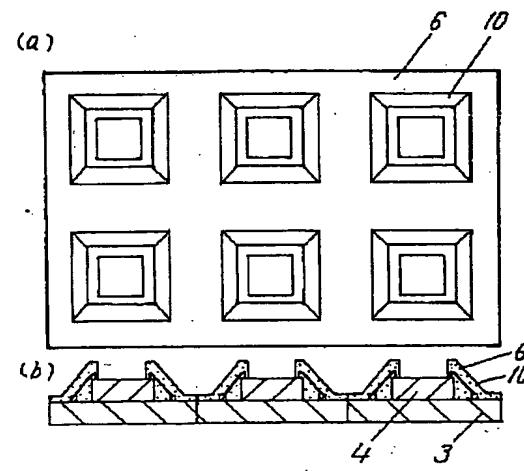
【図19】



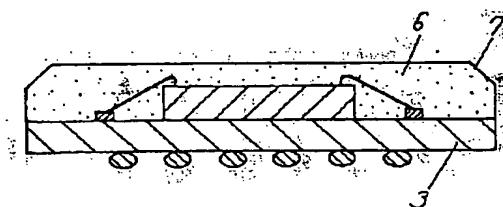
【図20】



【図21】

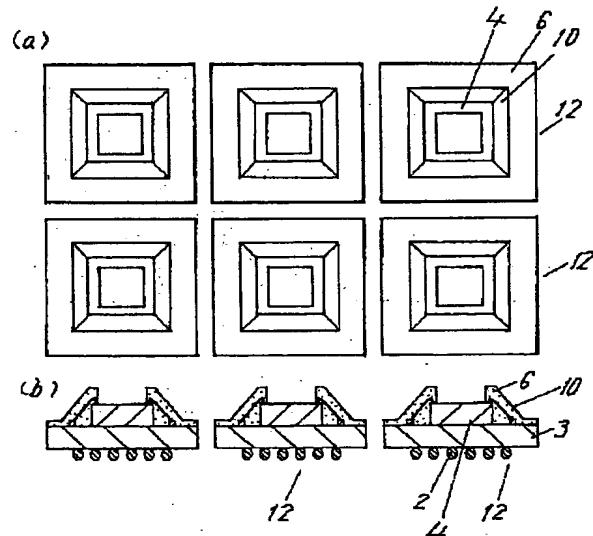


【図26】

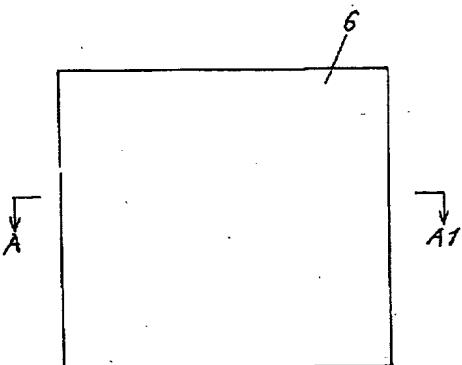


(14)

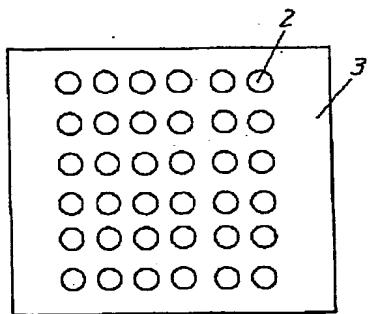
【図22】



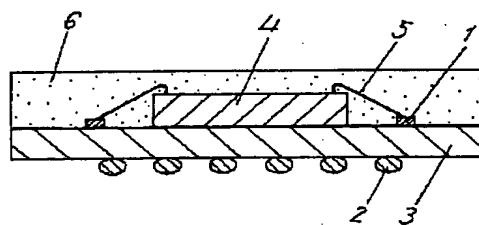
【図23】



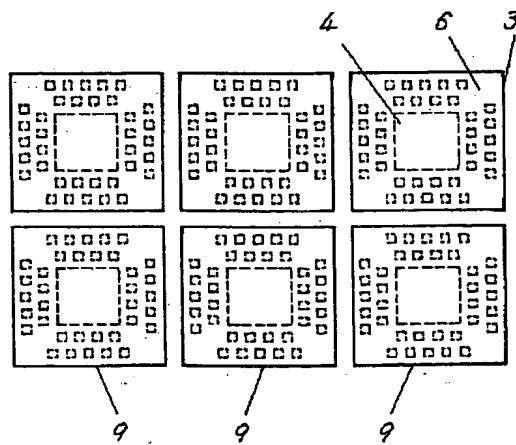
【図24】



【図25】

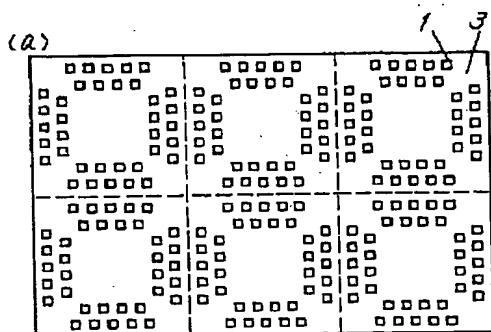


【図30】

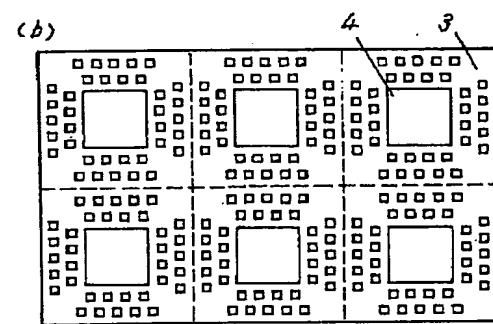
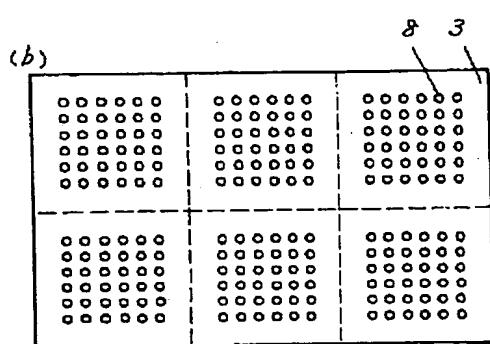
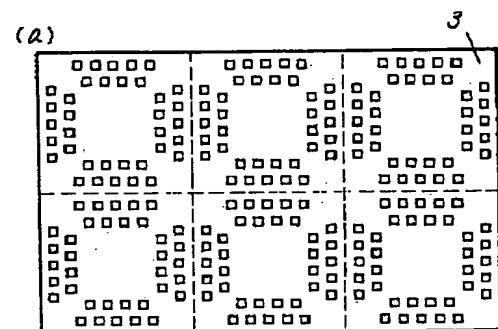


(15)

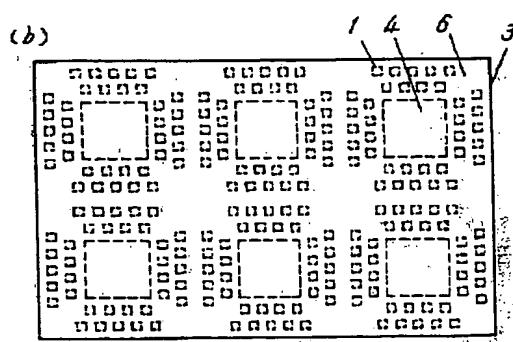
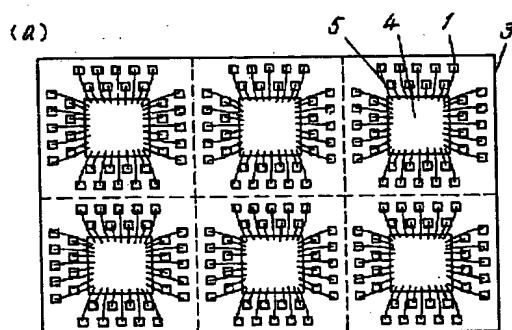
【図27】



【図28】



【図29】



(16)

フロントページの続き

(72)発明者 南尾 匡紀

大阪府高槻市幸町1番1号 松下電子工業
株式会社内

(72)発明者 福田 敏行

大阪府高槻市幸町1番1号 松下電子工業
株式会社内

(72)発明者 野村 徹

大阪府高槻市幸町1番1号 松下電子工業
株式会社内

Fターム(参考) 4M109 AA01 BA04 CA21 DA03

5F061 AA01 BA04 CA21 CB13